# The 21st IE (Intelligent Electronics) Competition

Ref. No. : Free 21-23 Topic : Free

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Members					
Title	A demonstration of Active Gate Drive Control for Three-phase Inverter:				
	Achieving Surge Voltage Reduction and Efficiency Enhancement				

### • Summary of the idea

This work presents a control method for fully digital active gate drivers to achieve both surge voltage reduction and efficiency enhancement in a three-phase inverter for motor drive applications.

The surge voltages of power devices during switching are generally influenced by the three-phase current values and their operating principles.

The proposed method adjusts the active gate driving patterns of six gate drivers according to the phase angle of the three-phase current to minimize the maximum surge voltage and switching losses.

A prototype three-phase inverter using a 6-in-1 SiC power module and six digital active gate driver ICs, was developed to verify the effectiveness of this control method.

### · Details of the idea

I. Introduction

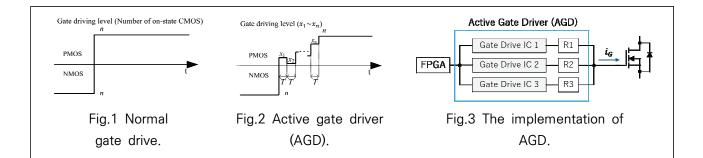
An active gate drive (AGD) technology is one of the key innovations to improve the trade-off relation between the surge voltage and switching loss of power devices in various power converters.

We have previously published the paper using specially laboratory-developed fully digital active gate driver IC with 63 CMOS drivers. In this competition, we will demonstrate a down-scaled model of 7-level AGD using commercially available gate driver ICs for three-phase inverter.

## II. Active Gate Control

Generally, the surge voltages of power devices in each switching are affected by the operation principle. In the proposed method, the active gate driving patterns of gate drivers are suitably changed (Fig.2) to minimize the highest surge voltage and the switching loss in a fundamental period of AC output.

In our demonstration, AGD can provide 7-level gate currents by using three general gate drivers selectively for each power device as shown in Fig. 3.



III. Laboratory-developed model

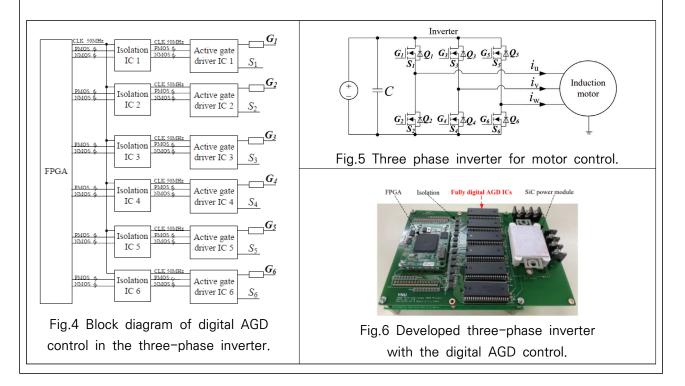
Fig. 4 shows the configuration of the fully digital AGDs and controllers where six fully digital AGD ICs are used to control six gate voltage, G1, G2, G3, G4, G5, and G6, in the prototype of the three-phase PWM inverter.

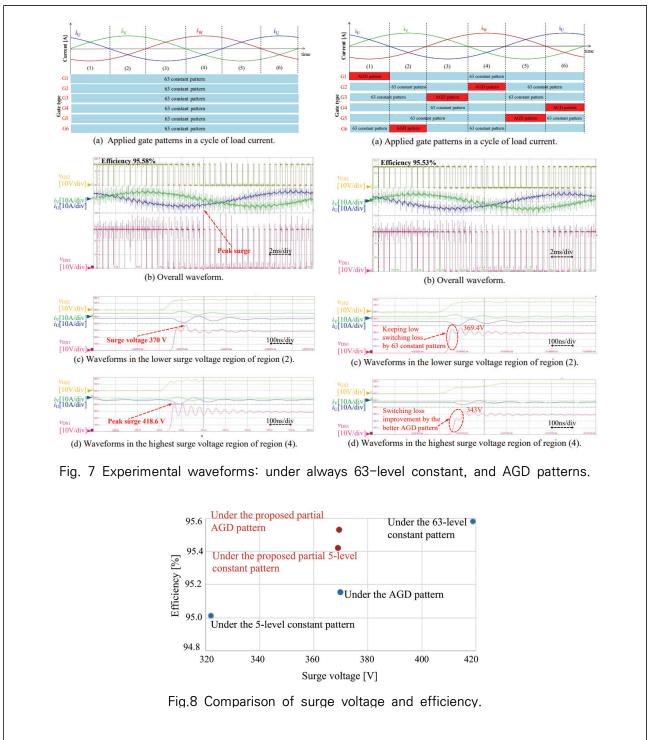
Fig. 5 shows the circuit diagram of a three-phase inverter. The G1 to G6 and S1 to S6 in Fig. 4 are connected to the gate and source terminals of six power devices Q1 to Q6 in a power module in Fig. 5, respectively.

Fig.6 shows the photograph of the laboratory-developed three-phase inverter with 63-level fully digital active gate driver IC for an induction motor.

As shown in Fig. 7, by applying the AGD control in the phase where peak serge occurred in 63-level constant pattern, the highest surge 418.6 V shown in 63-level constant pattern is suppressed to 343 V, while maintaining a high efficiency of 95.53%.

Fig. 8 shows the surge voltage and efficiency comparison based on the results shown in Fig. 7 and other patterns. It is seen that there is a trade-off relation between the switching loss and surge voltage reductions under the constant gate patterns and the always same pattern. This is the well-known limitation of the general gate drivers with the gate resistance adjustment. From the result, it is verified that the proposed partial AGD method improved the trade-off relationship.





### IV. Summary

We have revealed the effectiveness of AGD control in three-phase inverter as shown in above. We will demonstrate the waveforms of surge reduction and efficiency improvement by applying 7-level ADG to the three-phase inverter for induction motor in the competition.