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Topology and Control of a Seven-Level Converter based on Dual Four-Level Single Flying Capacitor

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ABSTRACT

This work introduces a novel seven-level inverter by incorporating a four-level single flying capacitor converter (SFCC) topology into the dual flying capacitor active-neutral-point-clamped (DFC-ANPC) prototype. A modified carrier-overlapped PWM technique has been developed to achieve natural voltage balancing for flying capacitors and the DC-link capacitors. The performance of the proposed topology and PWM method, rated at 1MVA power, has been demonstrated through simulation results. A comparative analysis between the proposed circuit and other 7L multilevel inverters (MLIs) has been conducted in terms of THD, power losses, and cost estimation.

1. Introduction

For medium- to high-power/voltage applications, shared DC-link multilevel inverters like NPC, FC, and MMC have gained interest for their ability to eliminate bulky and inefficient transformers and rectifiers [1]. However, costs, volume, and control complexity are increased by higher voltage levels due to more power semiconductors and passive components being required. Consequently, various novel MLIs topologies with fewer components have been proposed to address the challenge.

Hybrid MLIs (HMLIs) integrating basic configurations like H-bridge, NPC, T-Type, and FC show promise by leveraging advantages while mitigating certain constraints. For instance, dual FC ANPC (DFC-ANPC) inverters have been proposed by cascaded connected two parallel FC units with a HB cell, which improve power loss distribution and resolve voltage transient issues over in ANPC circuits [2]. However, as voltage levels increase, DFC-ANPC prototypes require more flying capacitors.

The paper proposes a new hybrid seven-level MLI based on the DFC-ANPC topology. The proposed circuit utilizes a four-level single flying capacitor (4L-SFC) inverter as the FC unit, requiring fewer switching devices and flying capacitors. Due to the lack of redundant switching states, a carrier-overlapped PWM (COPWM) strategy is implemented for the inverter, enabling the natural voltage balance of all capacitors. A 1MVA PSIM model verifies the proposed inverters' performance and PWM technique. Various comparative metrics, including THD, power losses, and cost estimation, have been employed to evaluate the proposed circuit against other 5L and 7L MLIs.

2. Proposed 7L-D4LSFC Topology and Control

2.1 Circuit Configuration

The proposed inverter is constructed by substituting the two conventional 4L-FC converters with 4L-SFC ones in the 7L DFC ANCPC circuit, as illustrated in Fig. 1. The 4L-SFC unit has only one flying capacitor, which is a significant reduction in the component count [3]. Furthermore, the total count of power IGBTs in the proposed inverter is lower than that in the DFC circuit, with 10 and 14, respectively. However, the inverter experiences unequal blocking voltages across these IGBTs.

Table I shows the switching states of the proposed inverter

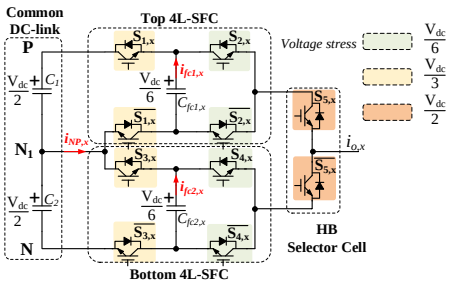


Fig. 1. Single-phase diagram of the proposed 7L-D4LSFC.

TABLE I. SWITCHING STATES EFFECT TO CURRENT DIRECTIONS AT FLYING CAPACITORS AND NEUTRAL POINT

$S_{1,x}$	$S_{2,x}$	$S_{3,x}$	$S_{4,x}$	$S_{5,x}$	v_{xN}	Switching states	FC Currents $i_{fc1,a}$	FC Currents $i_{fc2,a}$	NP Current $i_{NP,a}$
0	0	0	0	0	0	V_0	–	–	–
0	0	0	1	0	$V_{DC}/6$	V_1	–	$i_{0,a}$	–
0	0	1	0	0	$2V_{DC}/6$	V_2	–	$-i_{0,a}$	–
0	0	1	1	0	$V_{DC}/2$	V_{3N}	–	–	$i_{0,a}$
0	0	1	1	1	$V_{DC}/2$	V_{3P}	–	–	$i_{0,a}$
0	1	1	1	1	$4V_{DC}/6$	V_5	$i_{0,a}$	–	–
1	0	1	1	1	$5V_{DC}/6$	V_6	$-i_{0,a}$	–	–
1	1	1	1	1	V_{DC}	V_7	–	–	–

where the on and off states of each switch are indicated by “1” and “0”, respectively. The currents passing through flying capacitors and the neutral-point (NP) are also shown in the Table I.

2.2 PWM Method

Since the lack of redundant switching states, traditional modulation techniques are unable to meet the capacitor voltage balancing requirement. The COPWM technique, capable of generating (n-1) voltage levels within a sampling period (where 'n' represents the number of voltage levels), emerges as a promising option for the proposed inverter[4].

The COPWM pattern for four-level inverter is applied the top and bottom FC units of the proposed inverter, which is illustrated in Fig. 2. Whereas, the HB unit is operated under fundamental frequency as a selector cell.

2.3 Capacitor Voltages Control

The duty ratios for voltage vectors V1 and V2, as well as V5 and V6, are identical. Consequently, the current flowing through the flying capacitors during a sampling period remains at zero, which indicates that the PWM technique achieves natural balancing of FC voltages under ideal and steady-state conditions.

The NP current is influenced by voltage vector V_2, V_{3N}, V_{3P}, and V_4, then, the average value of the current for a single phase in a sampling period is calculated as.

$$i_{NP,x} = \begin{cases} \left(2 - 1/3 \cdot v_{ref,x}\right) \cdot i_{o,x} & 3 \le v_{ref,x} \le 6 \\ 1/3 \cdot v_{ref,x} \cdot i_{o,x} & 0 \le v_{ref,x} < 3 \end{cases} \quad (1)$$

Assuming that the reference voltage $v_{ref,x}$ and load current $i_{o,x}$ are sinusoidal and symmetrical, the average total neutral-point

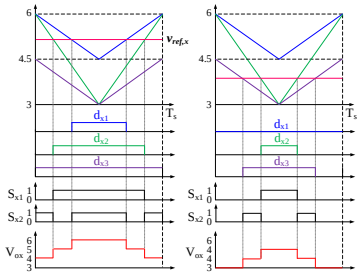


Fig. 2. PWM pattern, switching states, and output voltage generation of the top 4L-SFC unit.

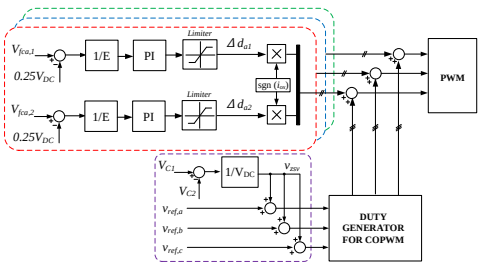


Fig. 3. Control block diagram for the capacitor voltages.

TABLE II. PARAMETERS FOR PSIM SIMULATION

Parameters	Values
Power rating	1 MVA
DC-link voltage	4.8 kV
Line-to-line voltage	3.3 kV
Fundamental frequency	60 Hz
Switching frequency	3 kHz
DC-link capacitors	1 mF
Flying capacitors	2 mF
Balanced Y-connected load	12 Ω/ PF=0.9
Deadtime	2 µs

current in a fundamental period is zero regardless of the modulation index and power factor. This indicates that the PWM modulation can achieve the balance of the DC-link capacitor voltages in a fundamental period under ideal and steady conditions.

In order to control the DC-link capacitor voltages under dynamic condition, a zero-sequence voltage, derived from the voltage mismatch between the two DC-link capacitors, is injected into reference voltages. Control of each flying capacitor voltage is achieved through a simple PI controller. The capacitor voltages control block diagram is illustrated in Fig. 3.

3. Simulation results and Comparisons

A 1MVA/3.3kV proposed circuit was built and simulated using PSIM, with simulation parameters detailed in Table II.

Fig. 4 shows the inverter's performance at unity modulation index. The THD of the line-to-line voltage and the output load current are about 16.6% and 0.6% respectively. All capacitor voltages are maintained at their reference values.

Comparisons between the proposed inverter and other topologies have been conducted. In Fig. 5, the proposed circuit exhibits comparable THD performance to 7L topologies at medium and high modulation indices.

The power losses analysis of these inverters under various output load powers, at MI=1 and 0.9 power factor, was shown in Fig. 6a. The power losses among these 7L inverters are negligible and notably lower compared to the 5L topology. Furthermore, Fig. 6b illustrates that the power losses of the proposed inverter are evenly distributed among its three units.

The cost of semiconductor devices, capacitors, and gating drivers are considered for these inverters. The proposed inverter has the lowest cost among these circuits, approximately 16% less than that of the 7L-DFC ANPC, as shown in Table III.

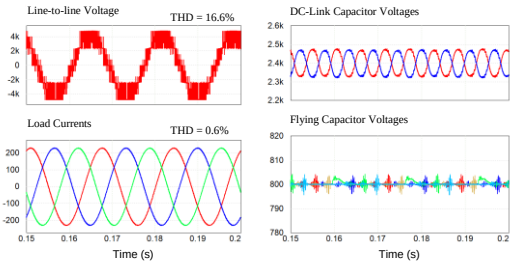


Fig. 4. Voltage and current waveforms at unity modulation index (MI = 1).

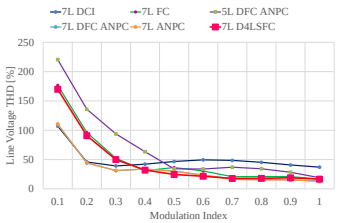
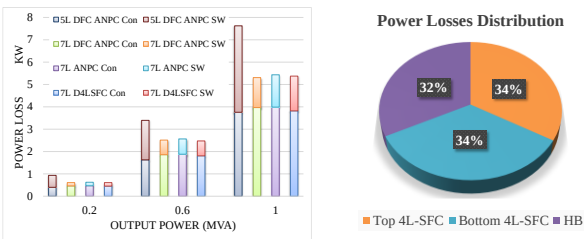


Fig. 5. Comparison of THD of line-to-line voltage.



(a) (b)

Fig. 6. Power losses analysis: (a) Power loss comparison at various output load power (b) power losses distribution of the proposed inverter.

TABLE III. COST COMPARISON (IN USD)

Devices	5L-DFC		7L-DFC		7L-ANPC		Proposed	
	no.	Price	no.	Price	no.	Price	no.	Price
Dual IGBT FF300R12KT4HOSA1	0	0	18	2,259	9	1,130	18	2,259
Dual IGBT FF300R17KE4	18	3,533	6	1,178	12	2,355	6	1,178
Capacitor B25680B0198K903	18	1,867	24	2,489	15	1,556	12	1,245
Gate driver SKYPER 32 R	18	1,786	24	2,382	21	2,084	24	2,382
Summation	**54**	**7,186**	**72**	**8,308**	**57**	**7,125**	**60**	**7064**

4. Conclusions

This paper has presented a new seven-level hybrid inverter topology based on the DFC ANPC prototypes for medium-voltage high-power applications. The proposed topology has been compared to other topologies in term of THD, power losses and device costs. The evaluation results show that the proposed topology gives a similar performance as that of the 7L topologies whereas the cost and size are reduced considerably.

References

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