약계통 조건 하에서 디지털 제어된 그리드 연계형 컨버터의 안정성에 대한 리뷰

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Review on the Stability of Digitally Controlled Grid-Connected Converters under Varying Impedance Conditions (Weak Grids)

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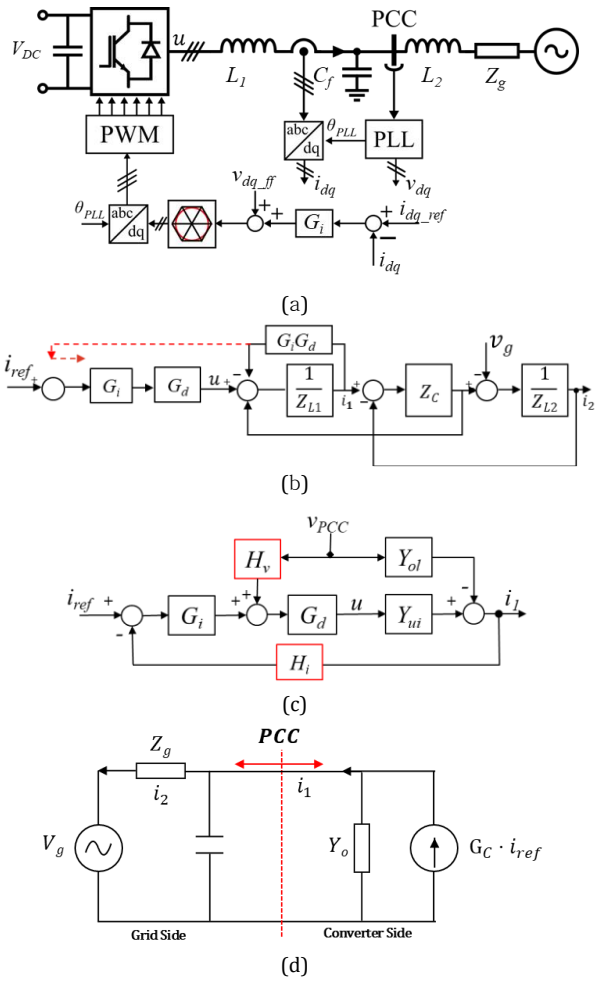
ABSTRACT

This review article explores the stability of digitally controlled grid-connected converters operating under varying grid or interconnection impedance. Due to global decarbonization policies and drives, renewable energy sources are becoming more integrated into the grid. Rising integration has resulted in a more complex and interconnected power system. This has caused the stability of grid-connected converters to be a critical issue, particularly since the continuous decommissioning of traditional synchronous generators (SGs) weakens the grid infrastructure. Interconnecting converters employ mostly digital control because it offers enhanced flexibility and precision in managing power flow. However, their harmonic stability under challenging grid conditions warrants careful examination. This article evaluates the stability challenges encountered by digitally controlled grid-connected converters in varying interconnection impedance environments.

1. INTRODUCTION

This review article refreshes the stability of digitally controlled grid-connected converters amidst fluctuating grid or interconnection impedance. The common control structure of voltage source converters (VSC) is depicted in Fig.1(a). The vector-controlled grid-following (GFL) converter is a well-adopted structure in both industry and academia. Not only does it provide simple and effective control means, but also versatility and resilience methods to tackle instabilities associated with the peculiarities introduced by the nature of digital control. The primary factors contributing to these instabilities are the control delay introduced by pulse width modulation (PWM) and the time required for control actions and sampling.

The proportional and integral (PI) controller provides a reliable means of current control in the rotating *dq* frame by regulating the inductor current and providing a virtual impedance employed in resonance damping of the VSC's output filters (LC or LCL). However, due to the time delay of the digital control, T_d, the virtual resistance emulated by the proportional current controller becomes negative in the frequency range above the critical frequency f_{crit}, of, $1/(4\,T_d)$ (i.e. $f_{samp}/6$), where f_{samp} is the sampling frequency [1]. This could jeopardize the stability of the control loop as it could introduce right-half-plane poles (RHP) and would exhibit nonminimum phase behavior if the resonance frequency f_r is greater than f_{crit}. Furthermore, the stability of the entire system can also be threatened, since the phase of the loop gain considering the time-delay impact tends to cross over 180° around the resonant frequency. However, this high-frequency harmonic instability can improve through the passivity-based design of converters; by imposing a nonnegative-real component in the VSC closed-loop output impedance Y_o. In other words, $Re\{Y_o(j\omega)\} \geq 0\}$. This can be evaluated qualitatively or analytically by examining a Bode plot to determine if the phase $\angle Y_o(j\omega)$ lies within the range of [-90°, 90°] for all ω ($\angle Y_o(j\omega) \in [-90°, 90°]$, ∀ ω). If this is



1: A generalized representation of a grid-connected converter system (a), the control block diagrams (b) & (c), and the closed-loop equivalent circuit.

satisfied, the VSC is said to be passive, and will not jeopardize the interconnected system [1]. This article reviews such known methods and their effectiveness.

2. CIRCUIT CONFIGURATION

Table 1: Parameter values of simulation

Parameter	Value	Parameter	Value
Vdc	400 V	k_p	3
V_{PCC}	220 V[50Hz]	k_i	2500
L_1 , L_2	0.4 mH	L_g	$0 < L_g < 7mH$
C_f	20 μF	f_r	2.5 kHz
f_{SW}	10 & 20 kHz	f_{samp}	10 & 20 kHz

The stability of a VSC is divided into internal stability, which entails reference tracking capability (this is dependent on the system loop gain and will not be discussed in this article), and external stability covers how the converter interacts with other connected systems (dependent on the closed-loop output admittance). For a converter to be internally stable, both gain and phase margin must be sufficient. On the other hand, external stability is not a necessary criterion. However, it is mandatory for enhanced harmonic stability.

Figure 1(a) is a converter side current-controlled GFL VSC connected to the grid through an LCL output filter network. From the topology, the small signal model in (b) and the equivalent representation in (c), which shows added stability enhancement measures H_v and H_i, can be derived, and finally, the representative circuit model in (d) can be presented. Through the impedance model, the effectiveness of the virtual impedance $Z_v = G_iG_d$ introduced by the current control loop is examined by rearranging the model as shown in Fig. 1(b). Thus,

$$G1_{Zv(s)} = \frac{i_2(s)}{u(s)} = \frac{Z_{C,i}}{Z_{L1}Z_{L2}+Z_{L1}Z_C+Z_{L2}Z_C+Z_{L2}Z_v+Z_vZ_C} \quad (1)$$

where $Z_C = \frac{1}{sC}$, $Z_L = sL$, G_i is a PI controller, and $G_d = e^{-1.5sT_s} = e^{-sTd}$ ($T_s = 1/f_{samp}$) is the combined PWM and sampling delay, It is clear from the bode plot of Fig .4 that the virtual impedance can be effective in resonance damping. However, it can also be seen that the low-frequency magnitude and phase response have been distorted by Z_v. Thus, a high integral gain would be required to ensure a high loop gain.

Similarly, based on the control diagram of Fig. 1(c), the converter plant model and open admittance are derived as follows.

$$Y_{ui}(s) = \frac{1}{Z_{L1}} = Y_{ol}(s) \quad (2)$$

Likewise, the loop gain, closed-loop gain and output admittance can be derived respectively as

$$T(s) = G_iG_dH_iY_{ui}(s) = Z_vH_iY_{ui}(s) \quad (3)$$

$$G_c(s) = \frac{Z_vY_{ui}(s)}{1+Z_vH_iY_{ui}(s)} \quad (4)$$

$$Y_o(s) = \frac{Y_{ol}(s) - H_vG_dY_{ui}(s)}{1+Z_vH_iY_{ui}(s)} \quad (5)$$

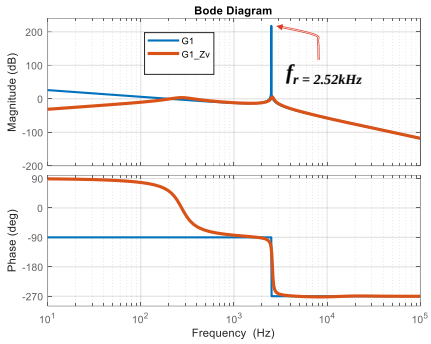


Fig. 2: Bode plot showing resonance damping by virtual impedance Z_v.

3. PASSIVITY-BASED STABILITY ANALYSIS

The interconnected system is passive if both the grid impedance and the converter output admittance are passive. Then the network is both passive and sufficiently stable. In order to access the passivity of the system, the high-frequency (HF) approximation is obtained as

$$G_i(s) = K_p + \frac{K_i}{s} \approx K_p \quad (6)$$

Then, considering $Y_{ui} = Y_{ol}$, the closed-loop output admittance is

$$Y_o(s) = \frac{Y_{ol}(s)(1 - H_vG_d)}{\frac{1}{Y_{ol}(s)} + \frac{1}{Y_{oa}(s)}}$$

$$= \frac{1}{\frac{1}{Y_{ol}(s)} + \frac{1}{Y_{oa}(s)}} - \frac{H_vG_d}{\frac{1}{Y_{ol}(s)} + \frac{1}{Y_{oa}(s)}} \quad (7)$$

Y_{ol} is passive (contains only filter components), However, Y_{oa}, is active. Also, the voltage feedforward element H_v, introduces an active offset term. Thus, the function H_v must be carefully selected. Now assuming $H_v = 0$, and H_i a non-negative constant, then

$$Y_{oa}(s) = \frac{1}{Z_vH_i}. \quad (8)$$

The HF response is

$$Y_{oa}(j\omega) = \frac{1}{K_pH_i}e^{j\omega T_d} = \frac{1}{K_pH_i}[\cos(\omega T_d) + j\sin(\omega T_d) \quad (9)$$

It is clear from (9) that the negative real part is dependent on ωT_d. It falls in the region (1/(4Td), 3/(4 T_d), namely, (f_{samp}/6, f_{samp}/2). This implies that due to the grid being passive, the VSC nonpassive region is in the region. The grid equivalent admittance is represented as

$$Y_g(s) = Z_c + \frac{1}{Z_{L2} + Z_g}. \quad (10)$$

On obtaining the bode plot for L_g = 2.6mH (f_{samp} = 10kHz) and comparing the phases as shown in Fig 3(a), the results are within expectation as the nonpassive region

is confirmed, with the phase of Y_o exceeding -90°. Similarly, although slightly different f_r, the simulation result is also within the region.

The straightforward way to enhance passivity is by reducing the control delay. This can easily be achieved

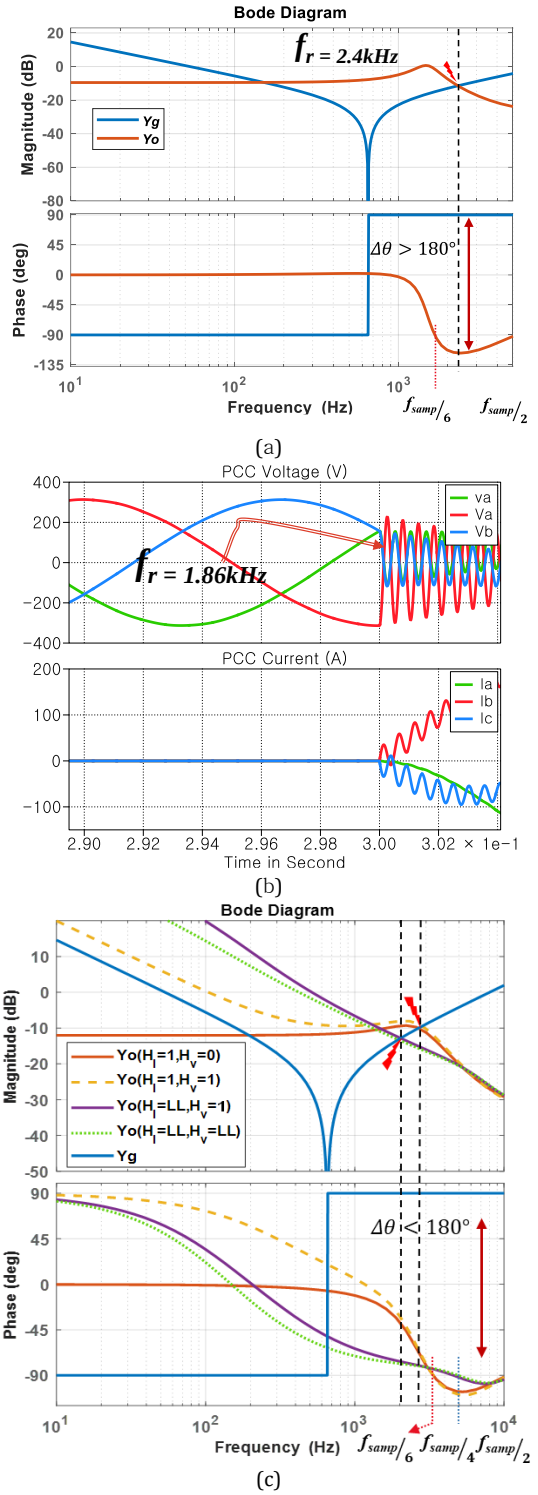


Fig.3: Bode plot showing the non passive region of the VSC (a), simulated result (b), passivity improvements steps (c).

either by reconsidering the PWM update type or simply increasing the switching frequency while keeping $T_d = 1.5\,T_s$ (T_s is now smaller) and thereby shrinking the nonpassive region. As can be verified from Fig. 3(c) (all variations of Y_o), increasing $f_{sw} = f_{samp}$ to $20kHz$ extends the passive region. However, steps to further extend this region can be taken to ensure a passive response even with weak grid conditions. For this purpose, variations of Y_o were analyzed as shown in Fig. 3 (c) where *LL* stands for lead−lag compensator.

As inferred in (7), the choice of H_V and H_I could improve or further deteriorate the harmonics and overall stability of the system. For the choice of $H_V = 0$, the output admittance is passive with a robust phase portrait up until around $f_{samp}/3$ (3.3kHz). However, a choice of 1, keeps the same passive region but with a much worse phase portrait resulting in worse harmonic stability. On the contrary, the voltage feedforward improves disturbance rejection, thus should be kept, and improved on. A logical choice is a lead-lag compensator to compensate for the digital delay (extending the passive region) and improve the phase portrait. Thus, both H_V and H_I are set as such.

$$H_i(s) = \frac{K_{pi}(s + \omega_{ai})}{(s + \omega_{bi})}, \qquad (11)$$

and

$$H_v(s) = \frac{K_{pv}(s + \omega_{av})}{(s + \omega_{bv})} \qquad (12)$$

The design approach is not straightforward; however, insight can be obtained from the authors in [3]. Thus, it should be designed to aid both system compensation and improve dynamic response. As such, Y_o is analyzed once more considering the effects of both. From Fig. 3(c) (Purple) it is clear that H_I has not only improved the phase portrait but also extended the passive region to as much as $f_{samp}/4$ (5kHz). Similarly, H_V improves the phase portrait in the lower region(dotted green).

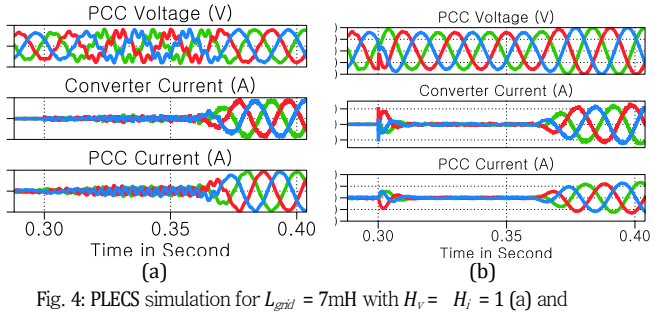


Fig. 4: PLECS simulation for L_{grid} = 7mH with H_V = H_I = 1 (a) and $H_V = H_v(s)$ and $H_I = H_i(s)$ (b).

Figure 4 validates the analysis on the importance of H_V and H_I. As can be seen, when a unity feedforward was applied, the converter harmonic stability deteriorates in comparison to when the lead-lag compensator is utilized.

4. CONCLUSION

In this article, we have reviewed the harmonic instability due to digital control of VSC. Further, we reviewed possible solutions and their kickbacks.

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