IFX Gen2 SiC MOS increases EV Charger performance compared with Gen1 SiC MOS.

KM LEE

The CoolSiC generation-2 (Gen2) Introduction (Page 3-13)

Striving for excellence in SiC MOSFETs

Building on the strenghts of Generation 1 to enable the accelerated design of more cost optimizated, efficient, compact, and reliabile systems

- **CoolSiC™ Generation 1**
  - ➔ Established the **benchmark in efficient power conversion**
  - ➔ Solved the **gate oxide reliability** risk in SiC MOSFETs using a trench gate
  - ➔ Overcame common SiC MOSFET limitations in **control and drive**
  - ➔ Made **all industry-standard packages** available

Reliable performance

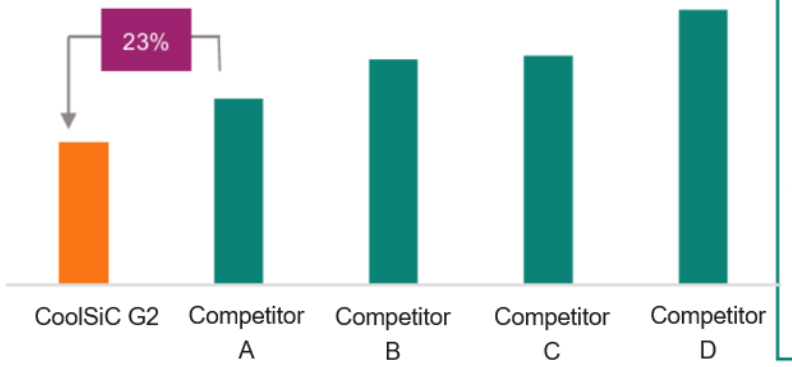
- **CoolSiC™ Generation 2**
  - ➔ **Enabling higher system performance per $**
  - ➔ **Maintaining Gen1 high reliability**
  - ➔ Adding **robustness and ease of use** features for **the highest design flexibility**
  - ➔ Advancing the **packaging technology for more output capability**

Unmatched industry leadership

CoolSiC gen2 shows the best FOMs to reach the highest performance and power density (25 °C comparison)

FoMs of competitor parts based on publicly available datasheets, 25°C, reference products:

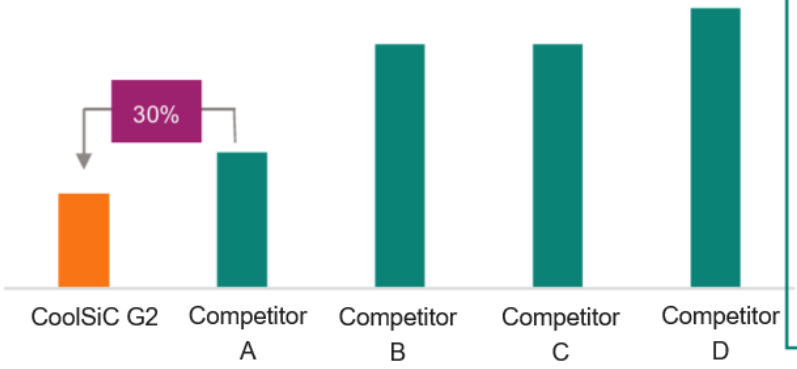
Qoss X Ron,typ @ 25°C



Lower Qoss → lower dead time, reduced circulating current in resonant topologies and less losses at high frequency. Enabler for HF ZVS topologies (e. g. > 250 kHz) **like LLC**.

Higher switching frequency, power density

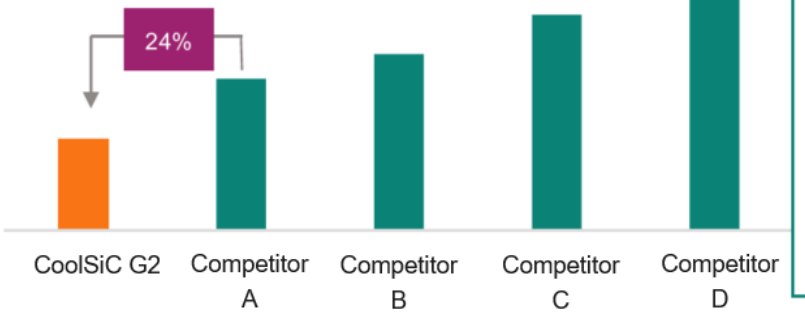
Qg X Ron,typ @ 25 °C



Lower Qg → reduced losses light load efficiency in soft switching topologies. Enables usage of gate drivers with lower current capability for same switching speed

Faster switching, more energy efficiency

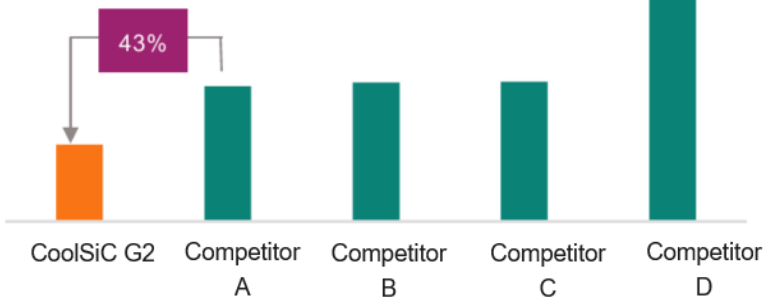
Eoss X Ron,typ @ 25 °C



Lower Eoss → Reduced switching losses in hard switched topologies. Better efficiency by lower magnetizing current possible
Best light-load efficiency

More energy efficiency and power density

Qrr X Ron,typ @ 25 °C



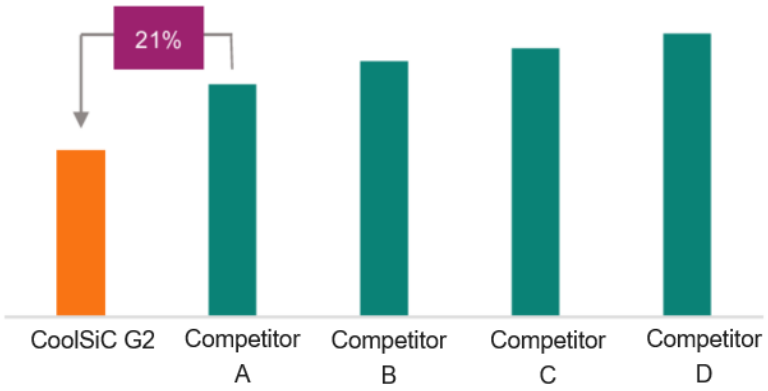
Lower Qrr → Enabler for hard switched half bridge topologies **(e. g. CCM Totem Pole PFC)**

Enables energy efficient designs

CoolSiC™ gen2 shows the best FOMs to reach the highest performance and power density (125 °C comparison)

FoMs of competitor parts based on publicly available datasheets, 125°C, reference products:

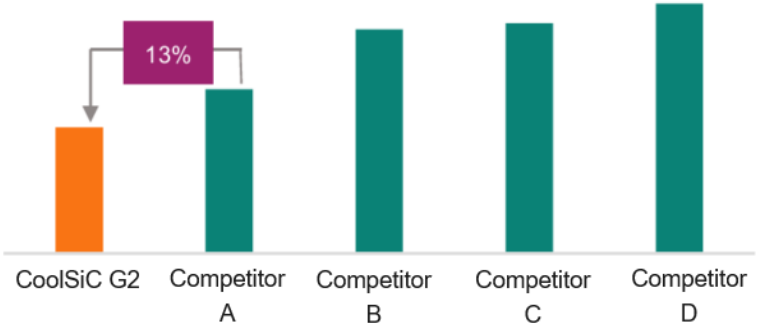
Qoss X Ron,typ @ 125°C



Lower Qoss → lower dead time, reduced circulating current in resonant topologies and less losses at high frequency. Enabler for HF ZVS topologies (e. g. > 250 kHz) **like LLC**.

Higher switching frequency, power density

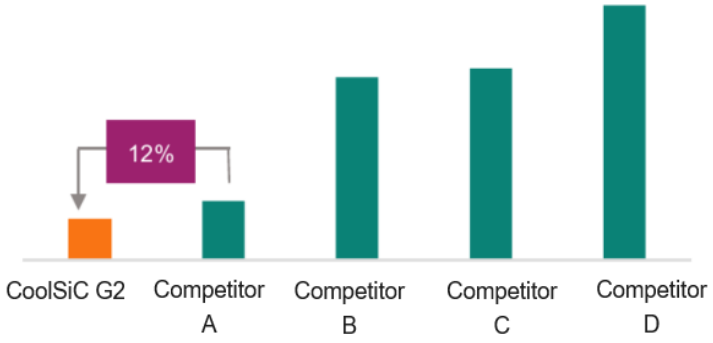
Eoss X Ron,typ @ 125 °C



Lower Eoss → Reduced switching losses in hard switched topologies. better efficiency by lower magnetizing current possible
Best light-load efficiency

More energy efficiency and power density

Qg X Ron,typ @ 125 °C



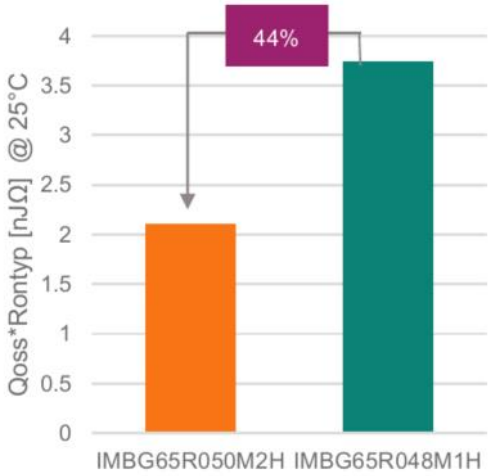
Lower Qg → reduced losses light load efficiency in HF resonant topologies. Enables usage of gate drivers with lower current capability for same switching speed

Faster switching, more energy efficiency

CoolSiC™ gen2 performance compared to gen1

G1 G2

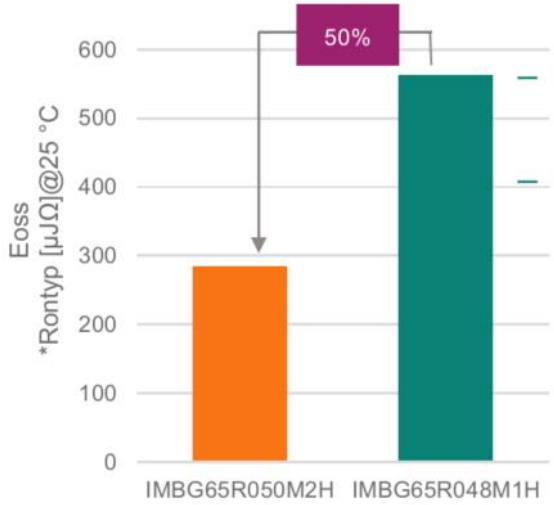
Qoss X Ron,typ @ 25°C



- Reduced Q_{oss} results in reduced current required for full ZVS.
- Reduced transition time for a given current.

Enabler for HF ZVS topologies (e. g. > 250 kHz)

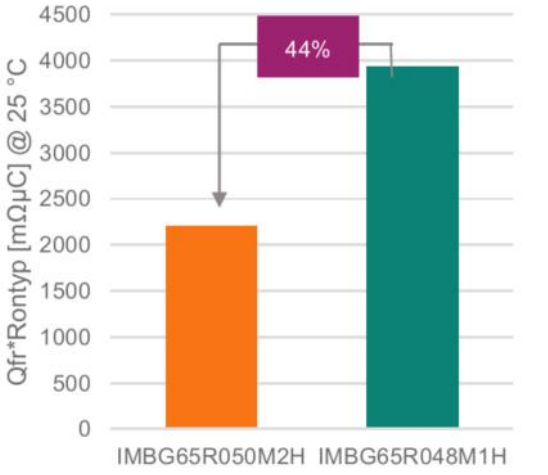
Eoss X Ron,typ @ 25°C



- Reduced E_{oss} results in reduced hard switching losses.
- Especially relevant in single ended topologies (e. g. Classic boost)

CoolSiC™ is effective also in single ended topologies

Qfr X Ron,typ @ 25 °C

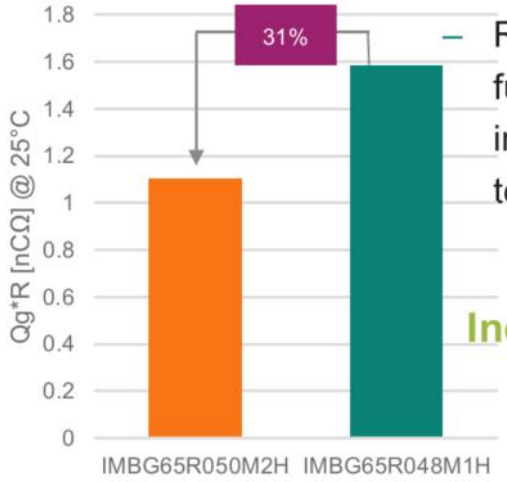


*Q_{fr} includes Q_{oss}

- Reduced Q_{fr} reduces switching losses and enables cycle by cycle hard commutation of body diode in totem pole like topologies.

Enabler for hard switched half bridge topologies (e. g. CCM Totem Pole PFC)

Qg X Ron,typ @ 25 °C

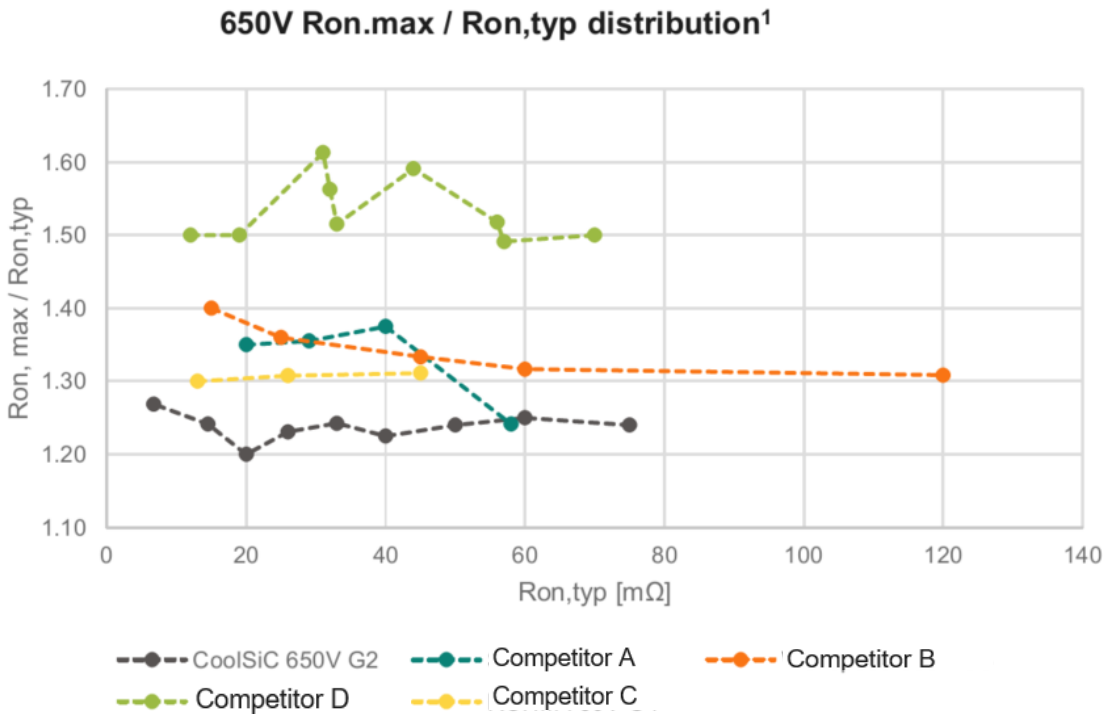


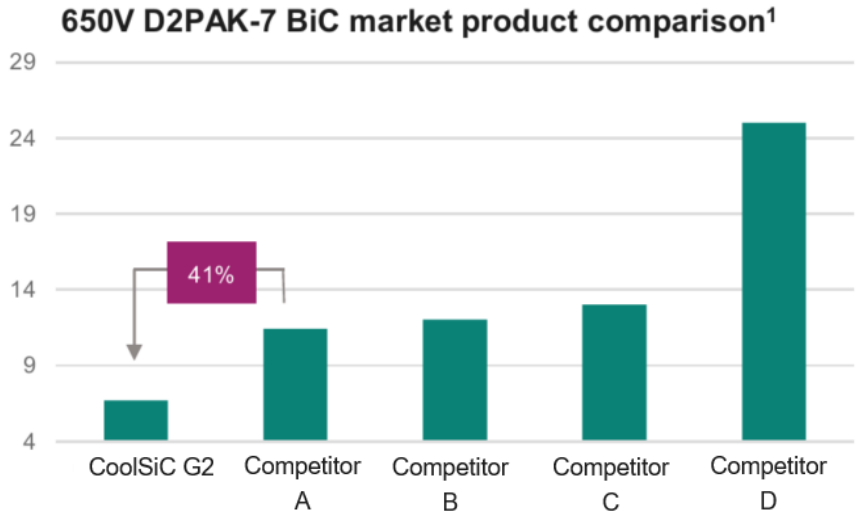
- Reduced gate driving losses help further improving light load efficiency in high frequency resonant topologies.

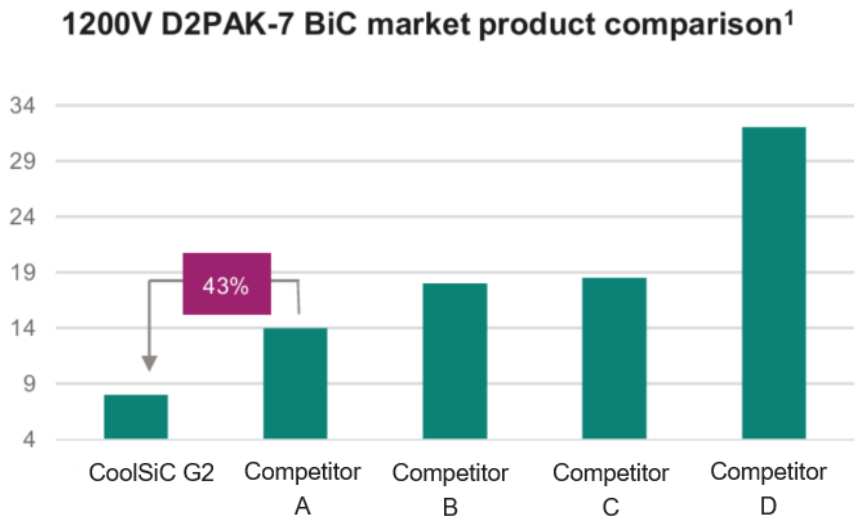
Increased light load efficiency in high frequency resonant topologies

CoolSiC™ gen2 boasts the lowest RDSon in SMD packages and the narrowest distribution

- CoolSiC™ G2 boasts the lowest Rdson in a standard SMD package (both in 650V and 1200V)
- It shows also the narrowest Rdson distribution

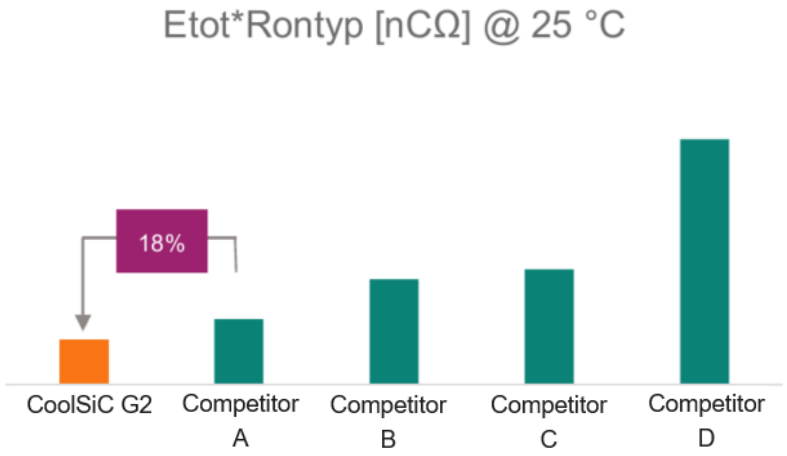






1) 650V and 1200V SiC MOSFET landscape as per Dec 2023. The 25°C values are reported

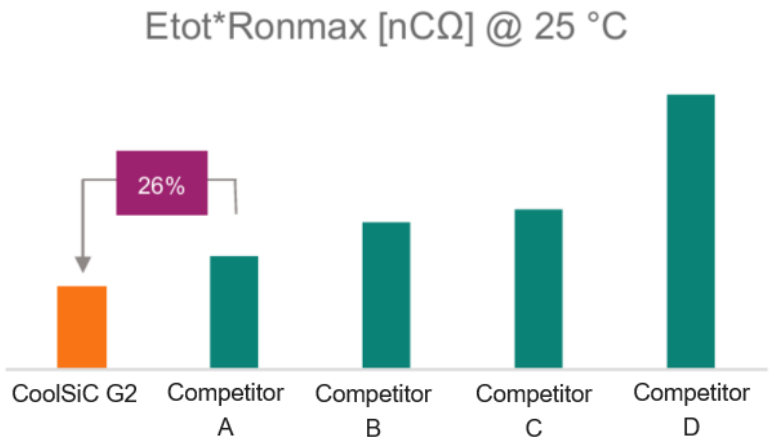
Low switches energies lead to lower power losses



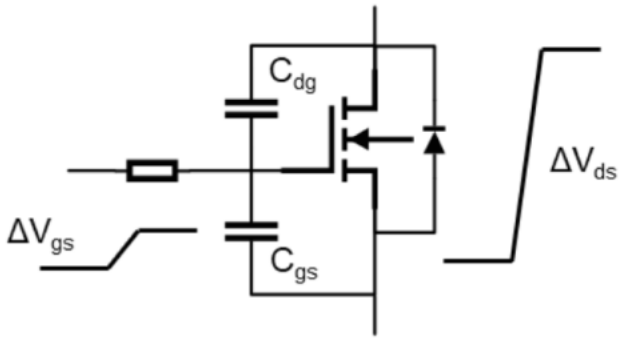
Lower Etot value enables lower power losses per installed Watt of system power

Test Condition
Infineon, IMBG65R040M2H (Vds=400, Id=22.9A, Rg=3.3 Ohms, Vgs = -5 – 18V)
Competitor A (Vds=400, Id=22.9A, Rg=3.3 Ohms, Vgs = -5 – 18V)
Competitor B (Vds=500, Id=20.0A, Rg=3.3 Ohms, Vgs = -4 – 18V)
Competitor C (Vds=400, Id=20.0A, Rg=3.3 Ohms, Vgs = -5 – 18V)
Competitor D (Vds=400, Id=20.0A, Rg=3.3 Ohms, Vgs = -4 – 18V)

Measurements in Infineon labs, with Datasheets

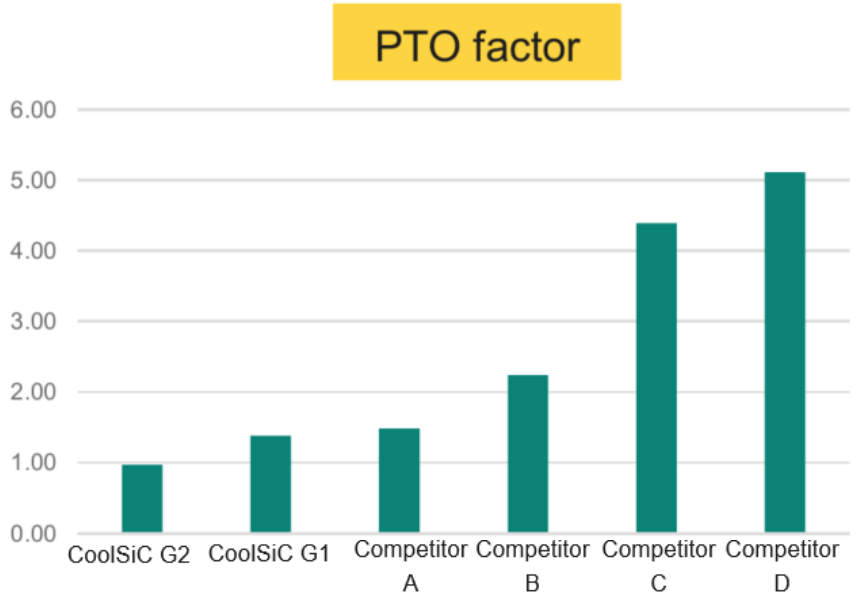


Best immunity against unwanted turn-on effects



- Parasitic (re)turn on (PTO) happens when the induced voltage on the gate is higher than the Vth – threshold voltage
- PTO may increase the turn-on losses

- The lower is the PTO factor, the less likely is to have parasitic turn on → higher efficiency and safer implementation of unipolar drive
- Both 1200V and 650V show excellent immunity against PTO. Below is reported, as example, a 650V / 750V PTO SiC MOSFET factor comparison

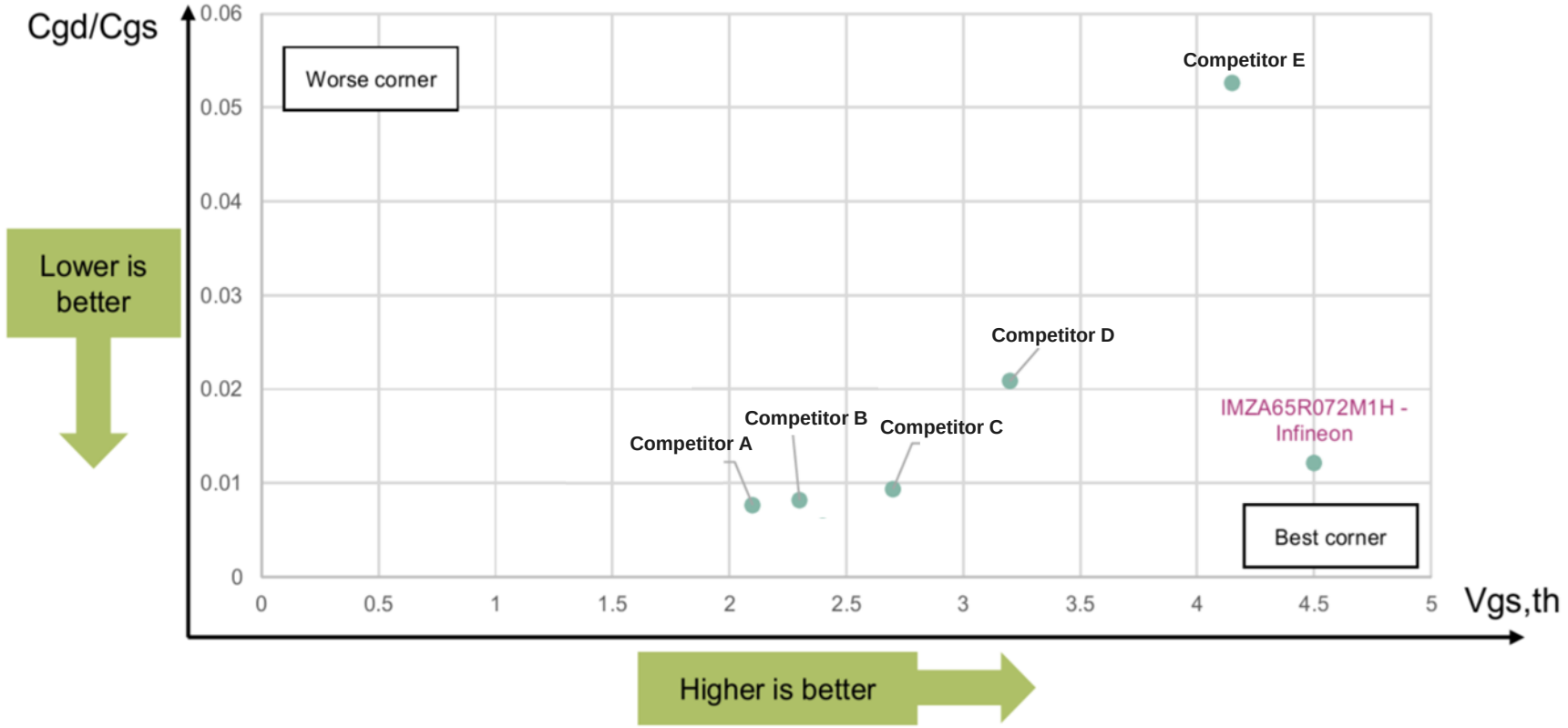


$$PTO\ factor = \frac{Q_{GD}@\ 400V}{Q_{GS}@Vgs_{(th)}25°C}$$

Note: PTO factor calculated from datasheets. The graphs reports the best devices among the ones analized

Why 0V turn off voltage is possible with negligible parasitic turn-on effects?

Datasheet comparison of 650V SiC MOSFET devices having a nominal on-state resistance of 60-80 mΩ.

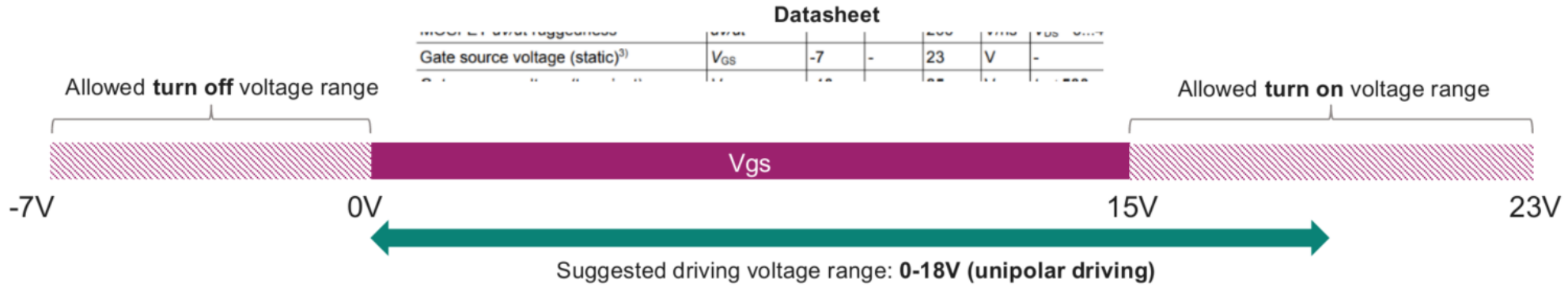


Best for reducing the parasitic turn-on:

- higher $Vgs_{(th)}$ – more margin against induced Vgs. The lower is the $Vgs_{(th)}$ the higher is the probability to have a return-on
- Lower capacitances ratio Cgd/Cgs – The lower is this ratio and the lower is the induced Vgs

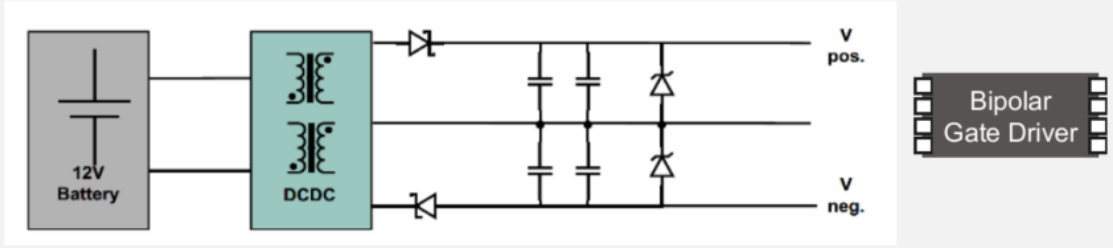
Putting the 2 results together, Infineon has *the best immunity against overall parasitic turn-on*

Flexible driving voltage

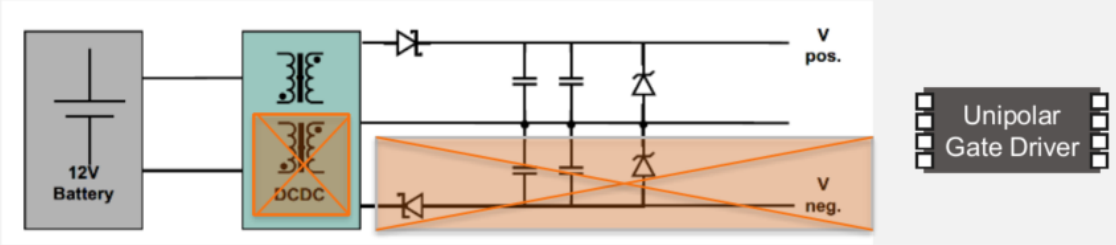


0V turn off voltage enables a more simplified and cheaper driving scheme

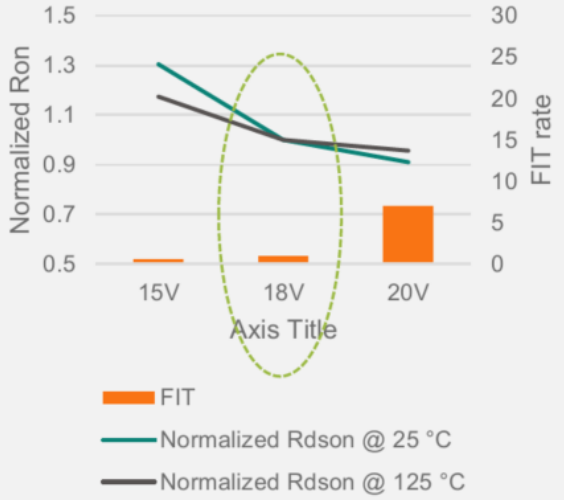
Negative gate voltage turn off



0V gate voltage turn off



18V turn on is the most optimized choice for performance, reliability and compatibility



- Rdson increases at 15V (by 17% @ 125°C)
- This behavior is the same for all SiC MOSFET brands
- FIT rates are very low also at 20V

**1 FIT = 1 failure expected per 10^9 device hours of operation (e.g.1M pieces over 1000 operating hours)

CoolSiC Trench MOSFET:
FoM comparison: Gen 1 vs Gen 2

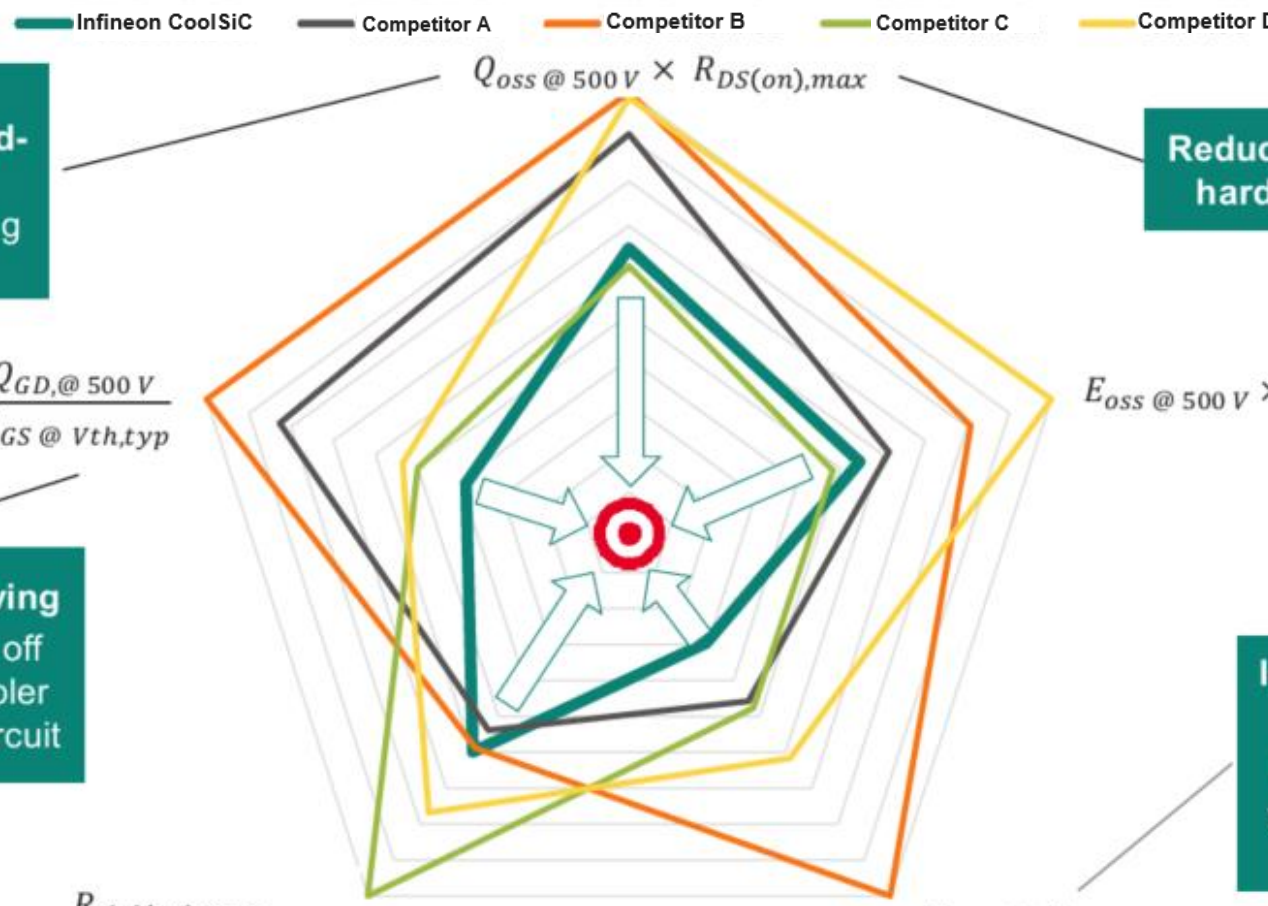
Parameter	IMZA65R057M1H 57 mΩ,typ Gen1	IMZA65R057M2H 57 mΩ,typ Gen2	Comparison (Gen2 vs Gen1)
Q_{oss} @ 400 V	65	46	~-30%
E_{oss} @ 400 V	9.8	6.5	~-35%
C_{iss} @ 400 V	930	695	~-25%
C_{rss} @ 400 V	11	6	~-45%
(C_{rss}/C_{iss}) @ 400 V	0.012	0.008	~-30%
$V_{(GS)th}$	Same target $V_{(GS)th}$ ~ 4.5V @ 25°C		~0%

Reduced switching losses

Reduced sensitivity to PTO*

- Gen1: datasheet values.
- Gen2: **characterization data based on EES with not final process**
- * parasitic return-on

CoolSiC™ is the most balanced technology combining ease of use, switching efficiency and superior thermal performances



Increased efficiency in the application through **reduced dead-time** and reduced circulating current in resonant topologies (e.g LLC)

Reduced switching losses in hard switched topologies

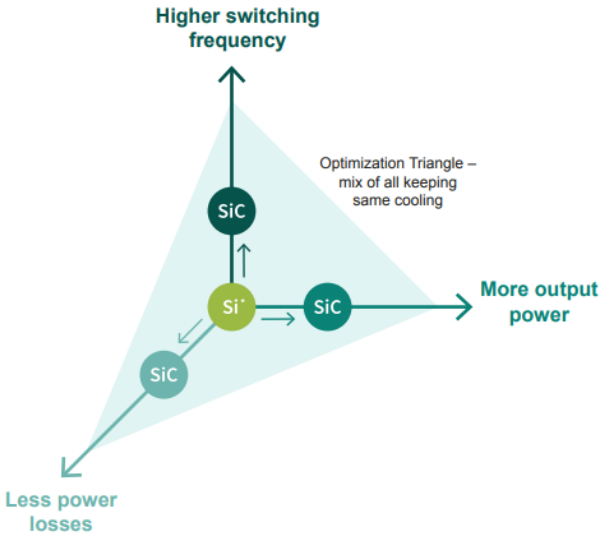
Enables unipolar driving
No need for negative off state voltages ➔ simpler and cheaper driving circuit

Increased light load efficiency
in soft switching topologies
Enables usage of gate drivers with lower current capability for same switching speed

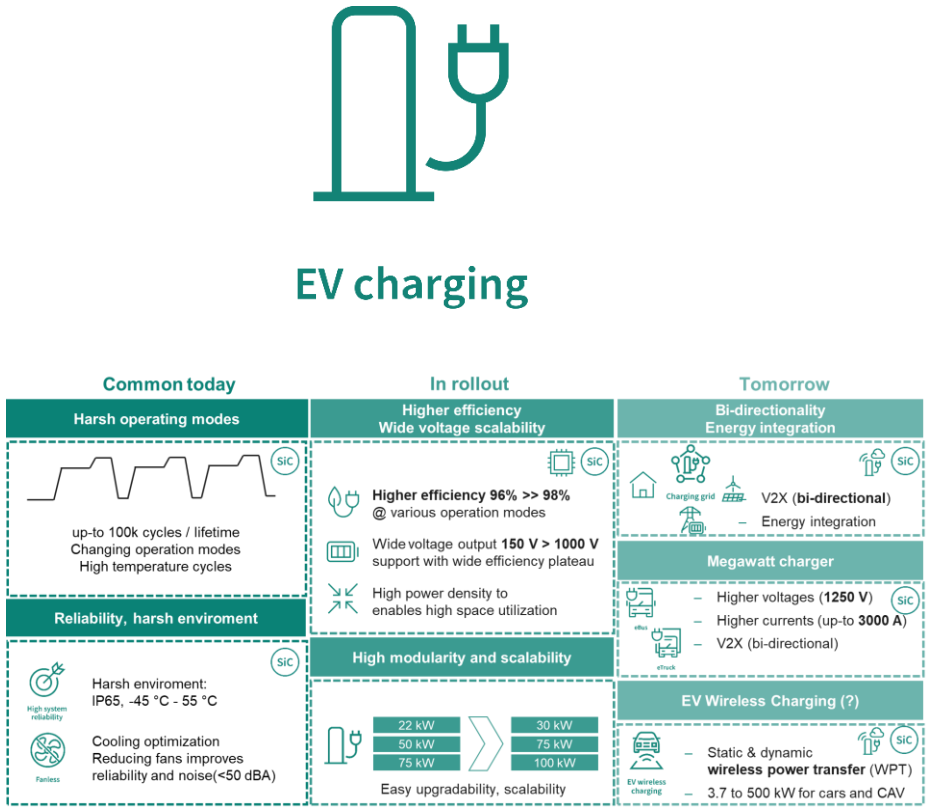
Increased power density,
more power for same package footprint

Gen1 vs Gen2 Efficiency Comparison in EV Charger's DCDC topology… (Page 15-28)

SiC power semiconductors are the perfect answer to many of today's and tomorrow’s DC EV charging requirements and trends

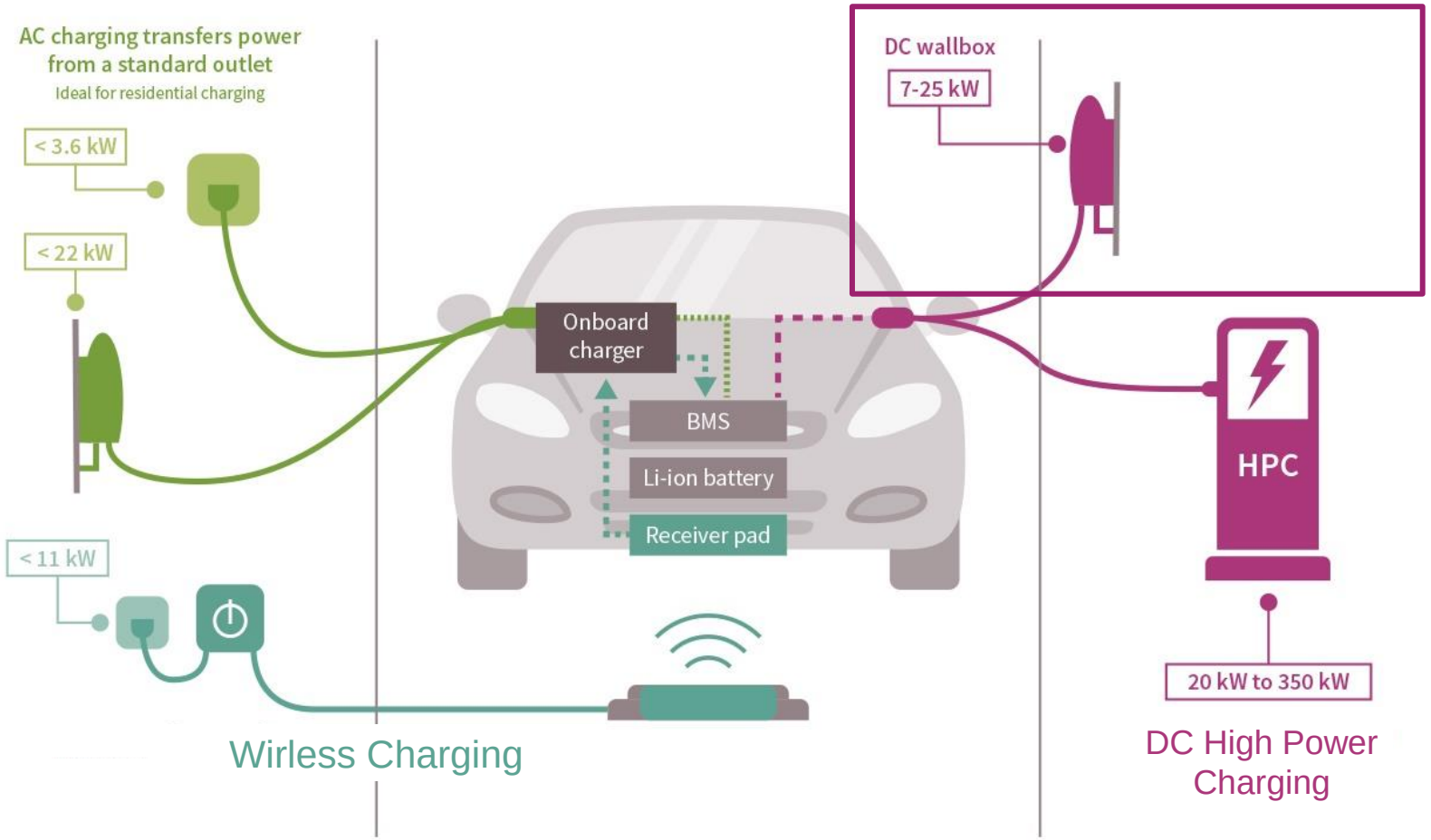


- Reduced system size
- Lower system cost
- Most efficient power conversion



EV charging is a key strategic application for Infineon
We cover the full ecosystem from AC to high power DC charging

Connectivity & Control | **Automotive systems** | **High power industrial systems**



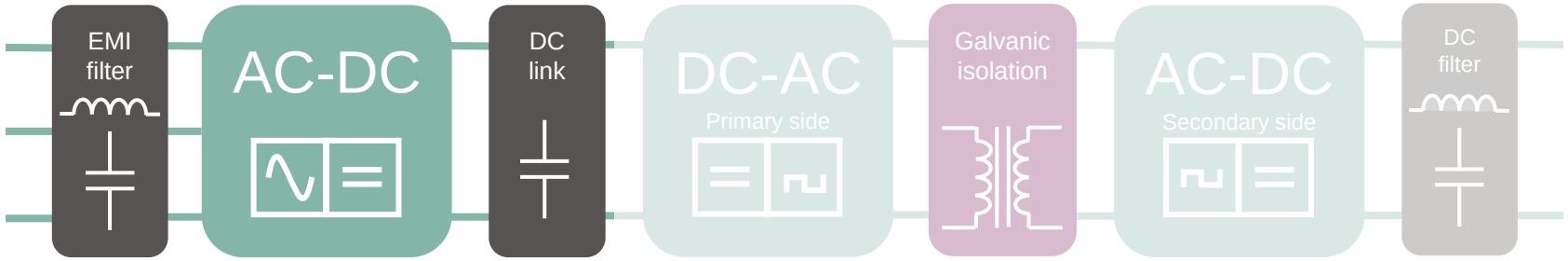
The focus use-case of our 22 kW reference design is a

bi-directional DC Wallbox

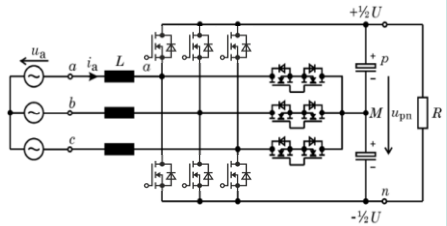
Infineon targets the complete EV charging ecosystem from AC to high-power DC

3 Level NPC2 and 2 Level 3phase are the most common PFC topologies for bi-directional DC EV Charging

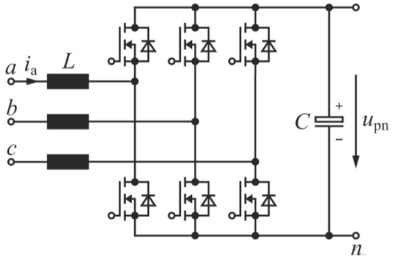
Most common PFC topologies for EV Charging



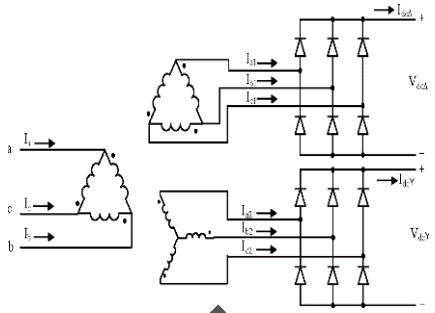
Vienna rectifier (uni-directional)



3L NPC2 (bi-directional)



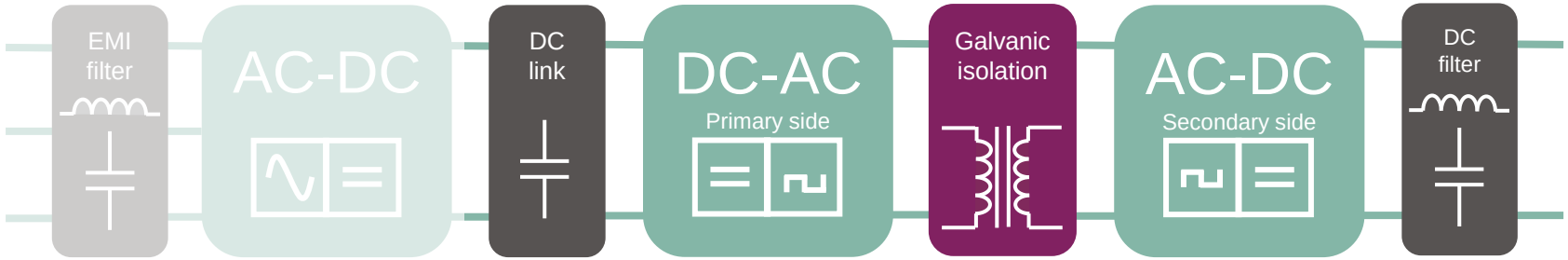
2L 3phase (bi-directional)

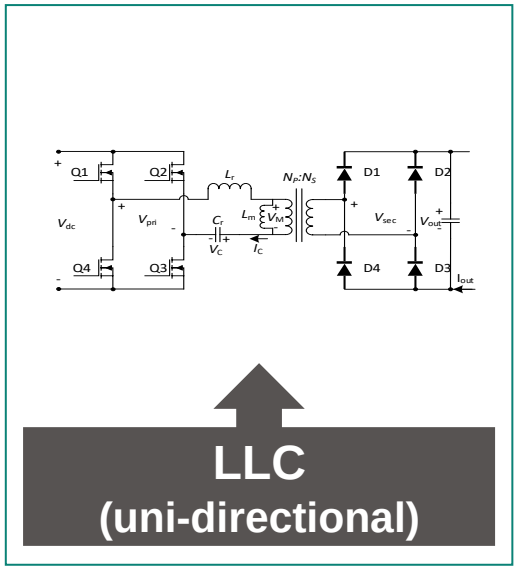


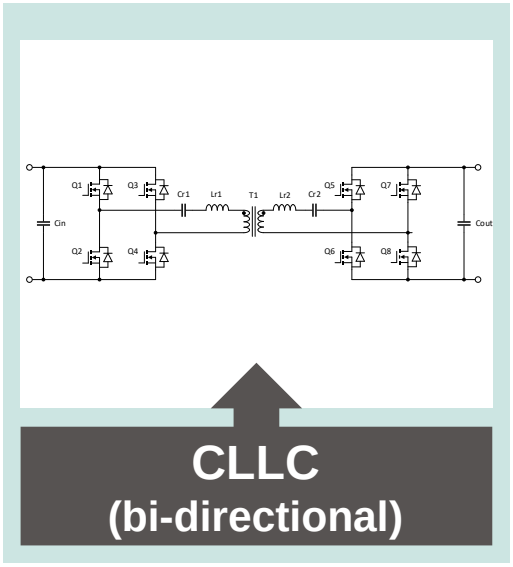
Diode rectifier

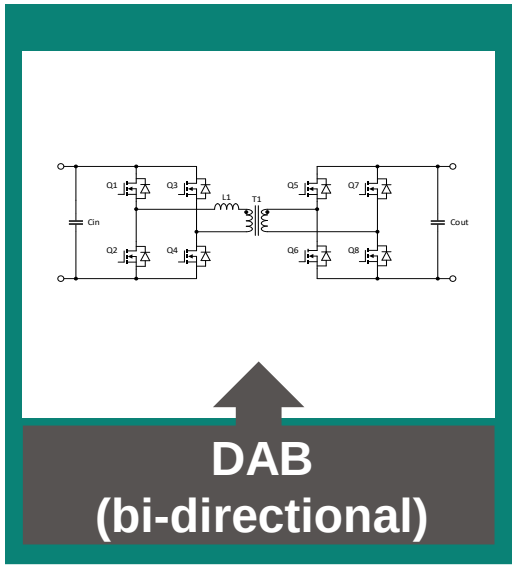
CLLC and Dual Active Bridge are the most common DC-DC power conversion topologies for bi-directional DC EV Charging

Most common DC-DC power conversion topologies for EV charging



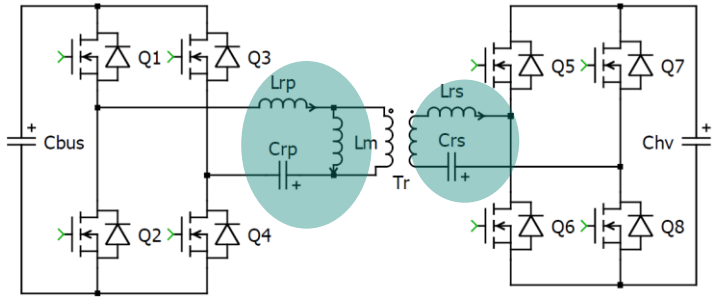






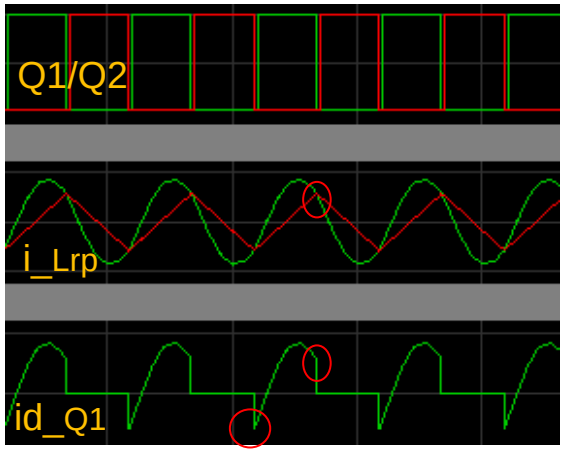
Comparison of full bridge CLLC and full bridge / 3-phase DAB: Hardware design

Full bridge CLLC

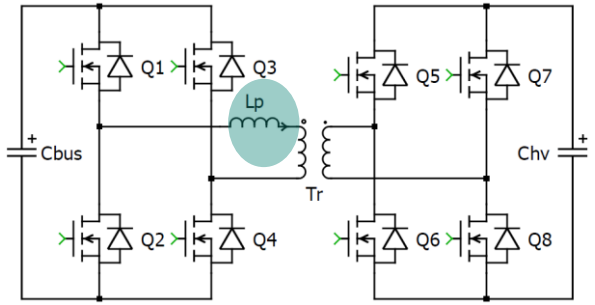


$L_{rs} = L_{rp}/n^2$, $C_{rs} = C_{rp} \cdot n^2$

PFM control:

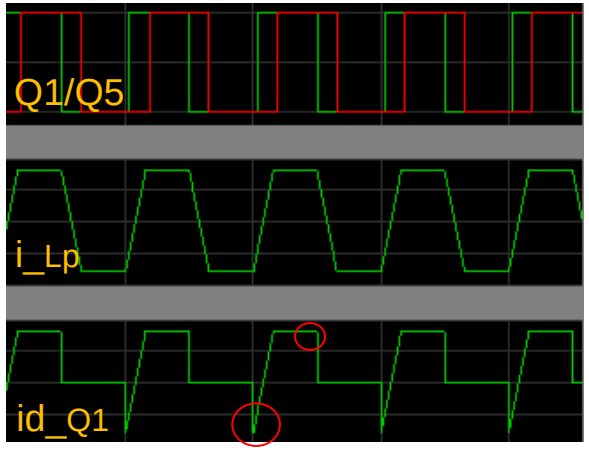


Full bridge DAB

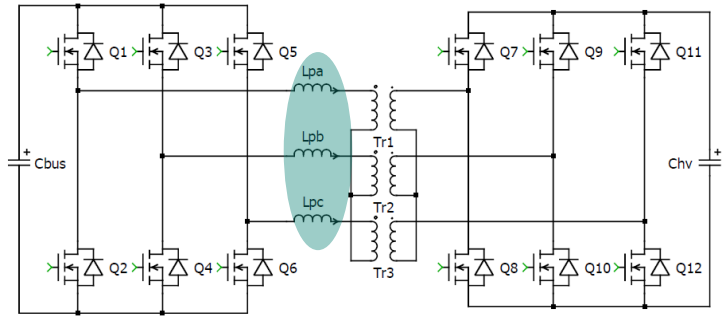


$$L_p = \frac{nV_{bus}V_{hv}D(1-D)}{2f_sP_o}$$

SPS control:

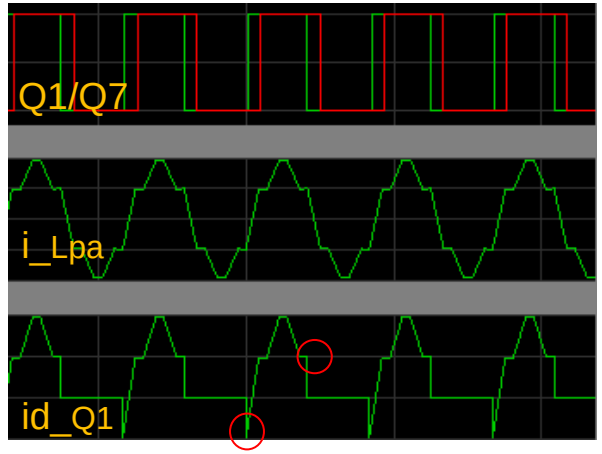


3-phase DAB (Y-connected)



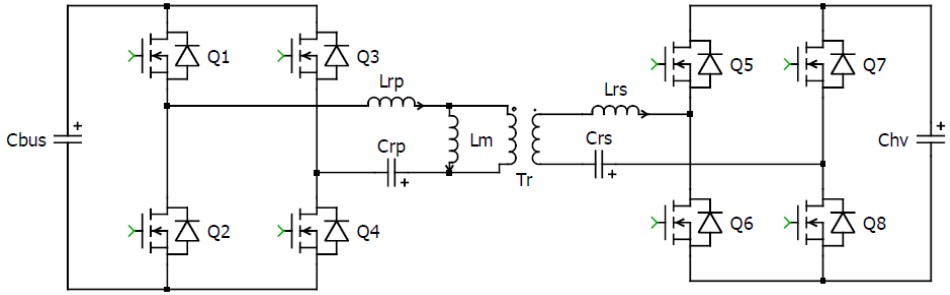
$L_{pa} = L_{pb} = L_{pc}$

SPS control:

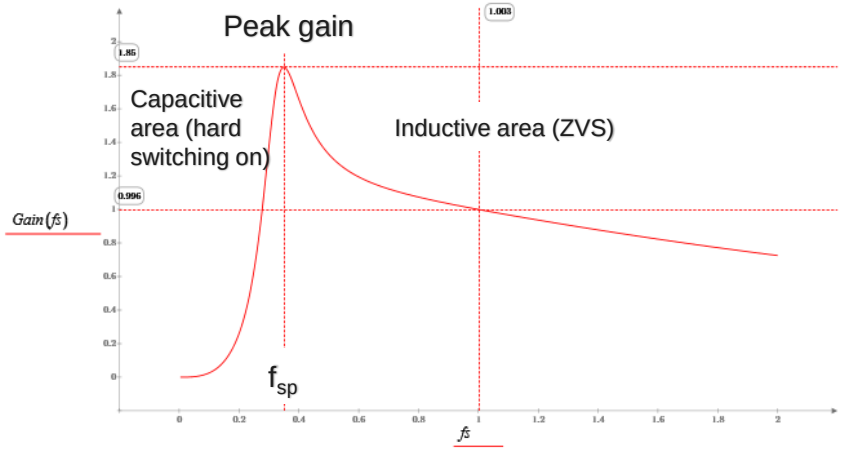


Full bridge CLLC ZVS (Zero Voltage Switching) region

Full bridge CLLC



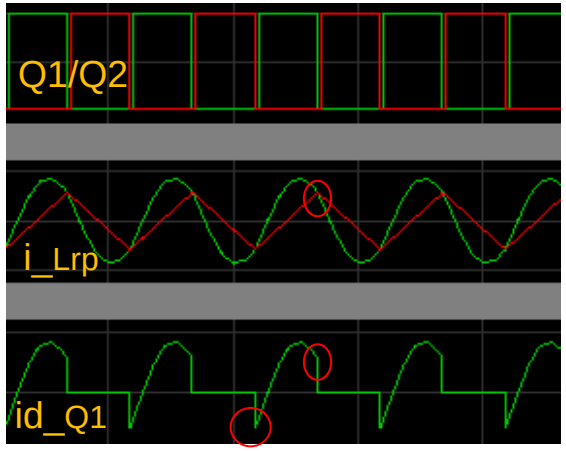
PFM control for CLLC, aims to control the voltage gain



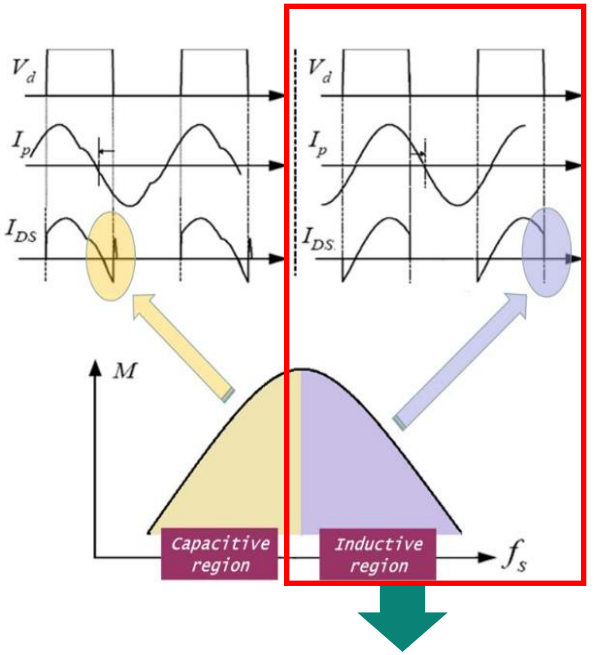
When $f_s > f_{sp}$, both the monopoly of voltage gain and ZVS of primary MOSFET can be achieved

CLLC Waveform

PFM control:



- EMI design: easy
- Flat efficiency curve
- Easy ZVS

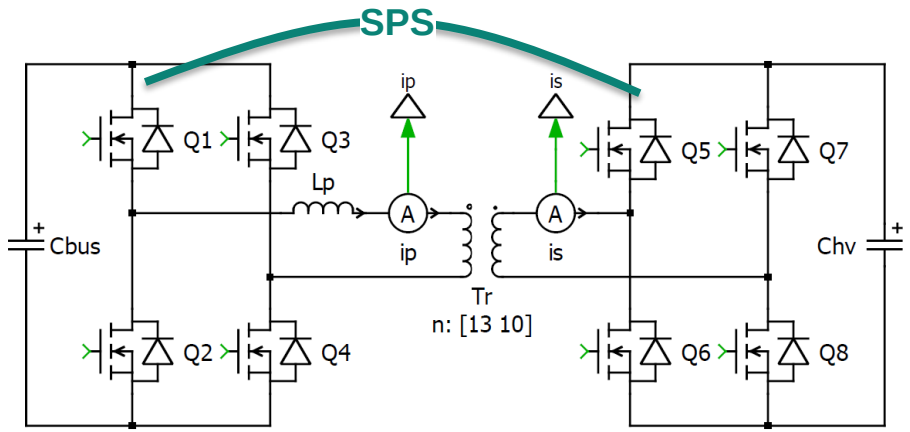


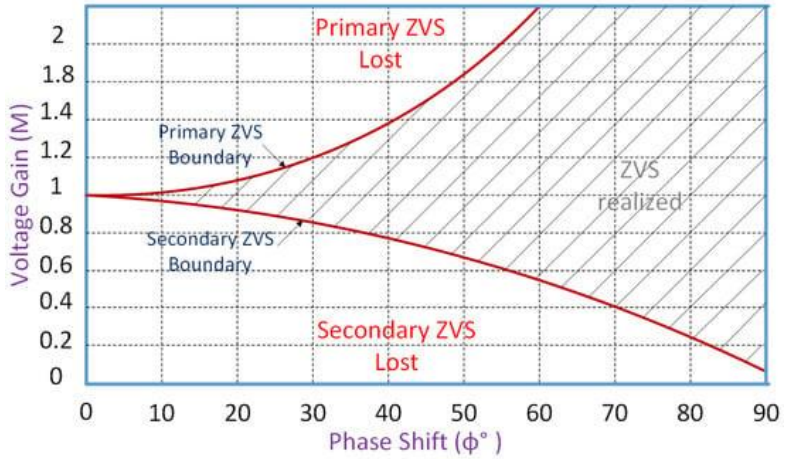
When turn on, ZVS (O)

When turn off, ZVS (X)

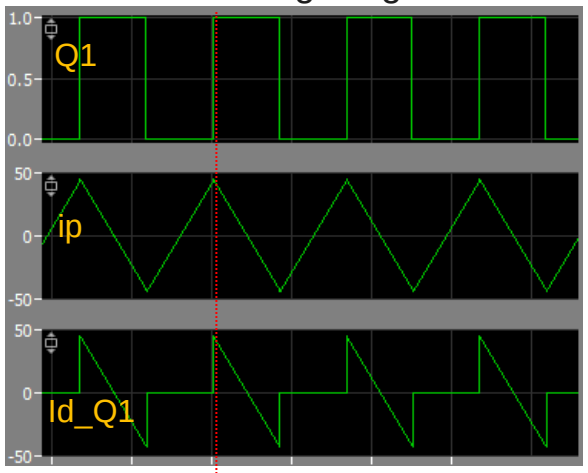
DAB Hard switching region

Fundamental challenge: DAB looses ZVS soft switching, according to ZVS boundary. Light load is worst for ZVS



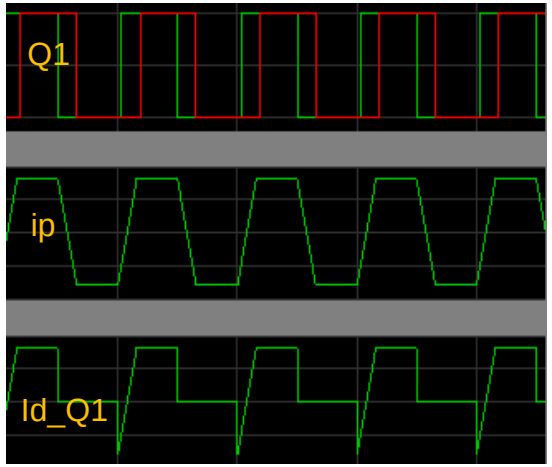


Hard switching in light load



No ZVS

Soft switching in ZVS boundary



Output voltage: 1000 V		
Output load	**0.5kW**	**15kW**
Turn-on current of Q1	43.3A	26.1A
RMS current of Q1	17.9A	20.7A
Losses of Q1	116W	76.4W

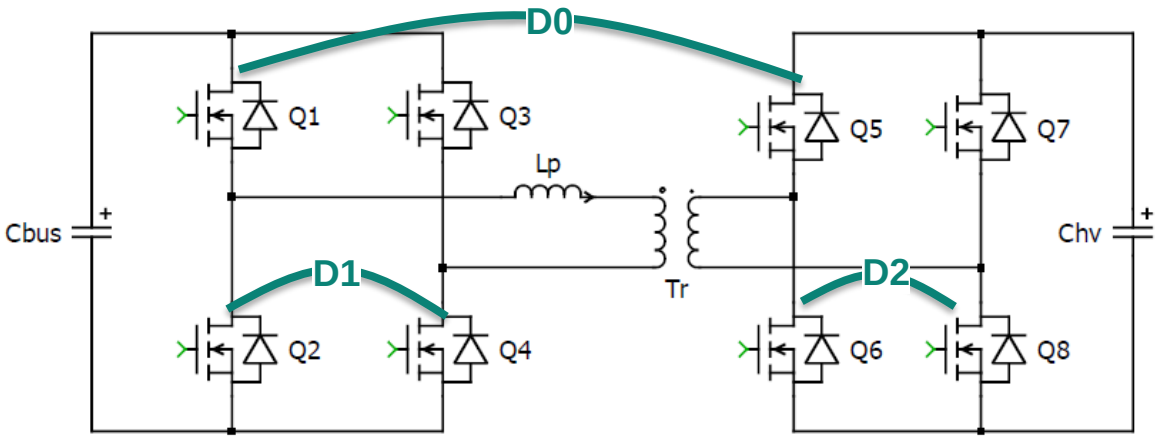
- Light load is the worst condition when $\boldsymbol{Vin \neq n \cdot Vo}$
- MOSFET can not endure the high loss at light load

Gen 2 will be best which has low switching loss to cover the wide load

Control concept for DAB and 3-phase DAB: New approach for control algorithm design

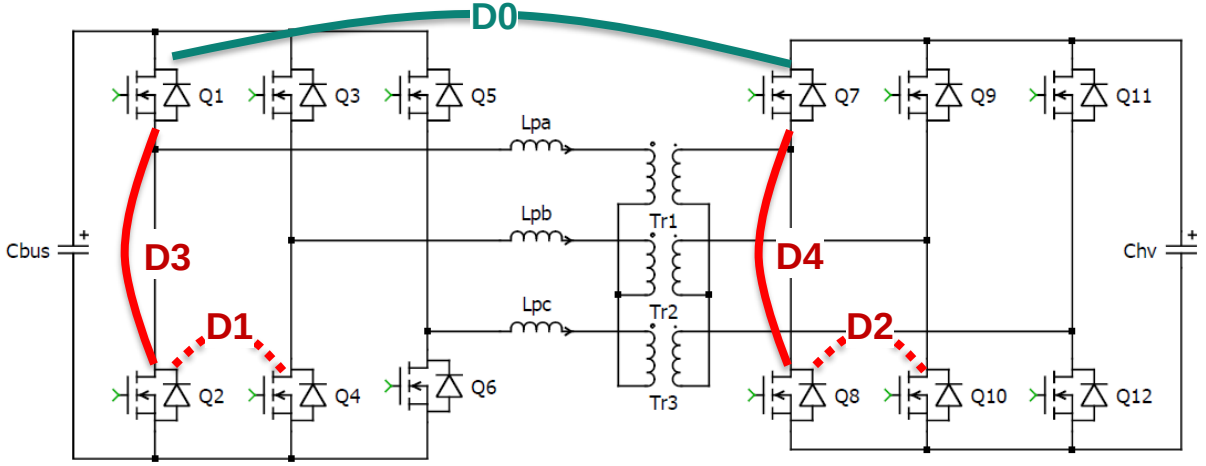
Solution: adopt more control freedom based on a reasonable optimization objective, for example minimizing the turn-on current

For full-bridge DAB



Control method	Control freedom	Degrees of control freedom
SPS	D0	1
DPS	D0, only D1or D2	2
EPS	D0, D1=D2	2

For 3-phase DAB



An intrinsic phase shift (D1/D2, 120°) already exists in 3-phase DAB

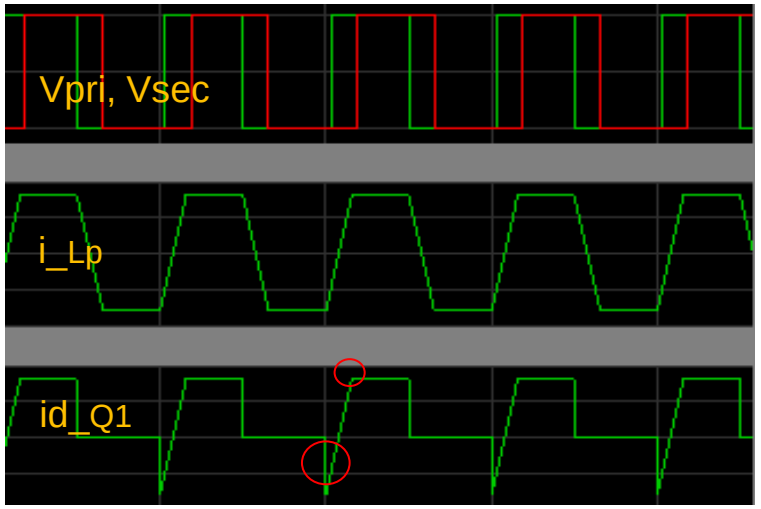
Control method	Control freedom	Degrees of control freedom	Applicable condition
IFX method #1	D0, D3=D4, symmetric PWM	2	Vin>n*Vo
IFX method #2	D0, D3=D4, complementary PWM	2	Vin<n*Vo

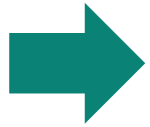
New approach : 2 control freedom + software simplicity

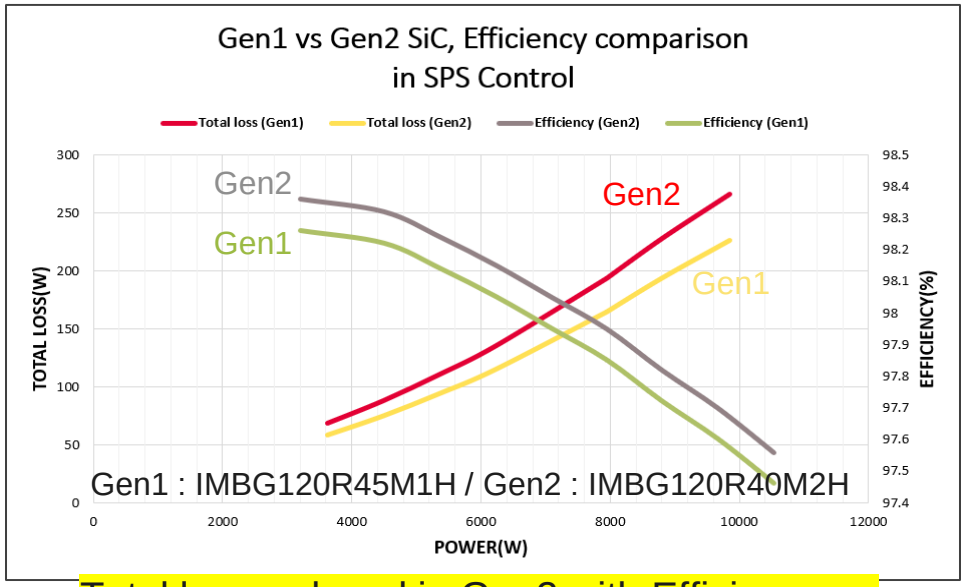
Control concept of DAB with Gen1 vs Gen2 SiC Efficiency Comparison

DAB SPS control

SPS control:



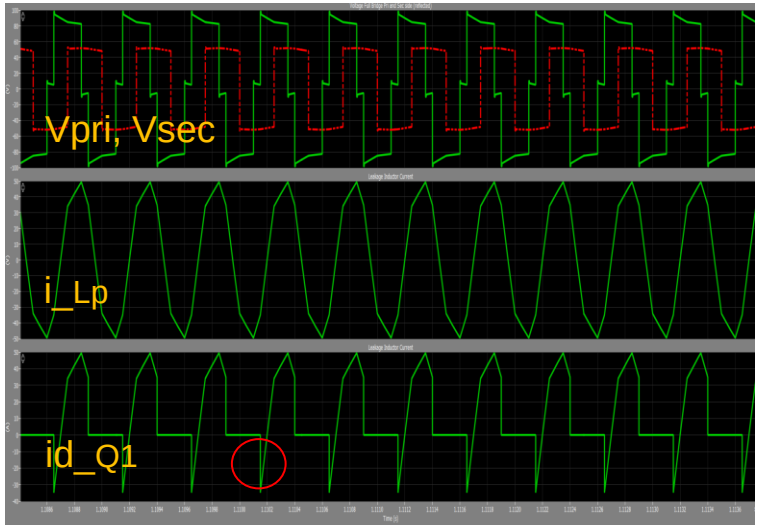


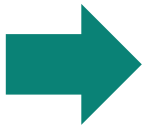


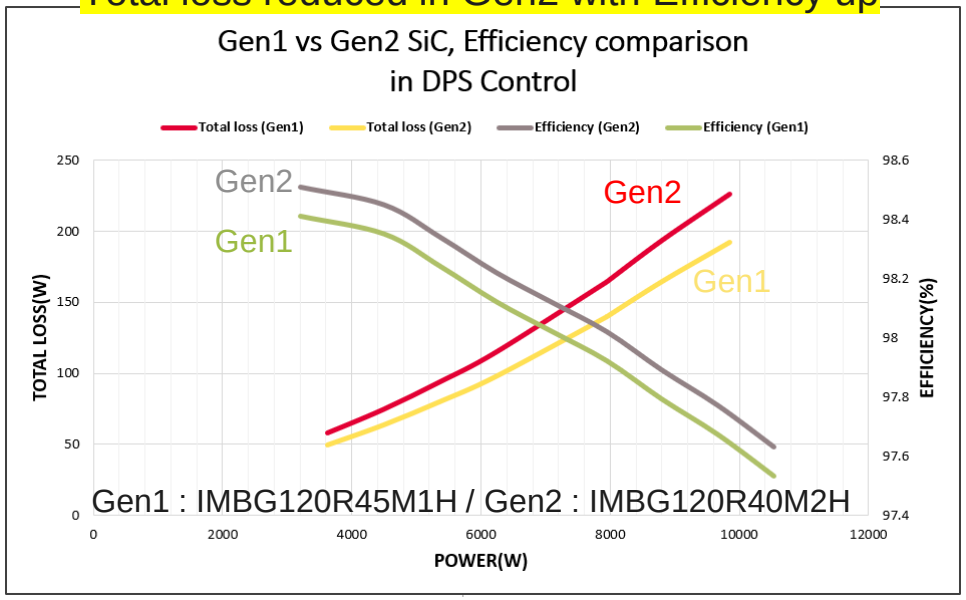
Total loss reduced in Gen2 with Efficiency up

DAB DPS control

DPS control:



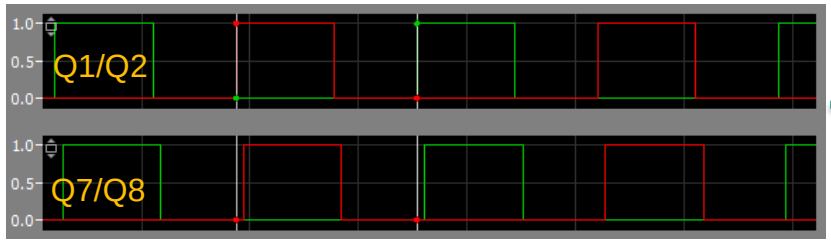


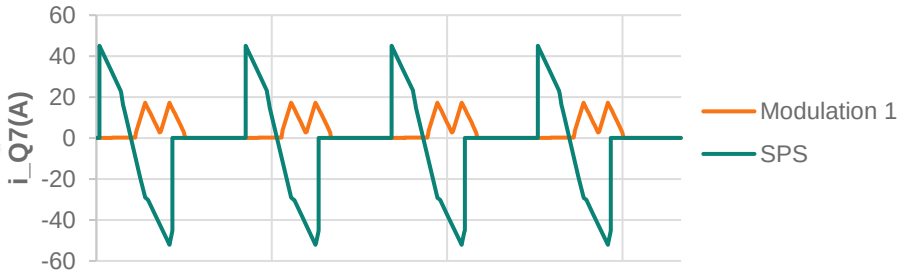


Control concept for 3-phase DAB: Implementation and results of new control algorithm

3-Phase DAB control

Modulation scheme 1: SPS + symmetric PWM
(D0, D3=D4, when $V_{bus} > n * V_{hv}$)

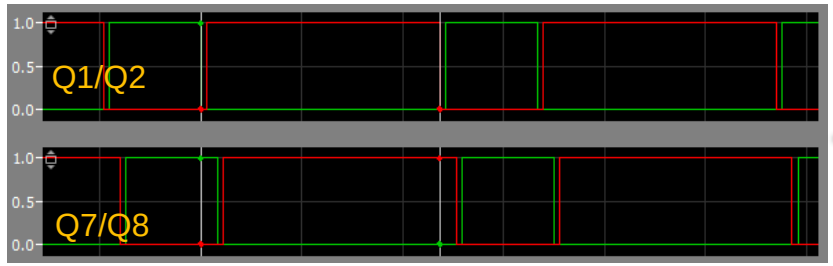


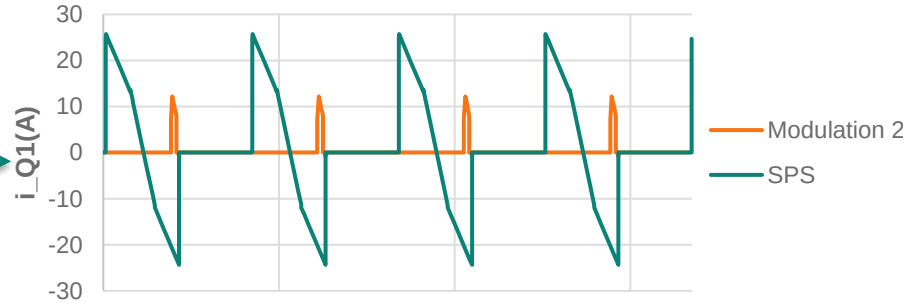


at V_{bus} = 680 V, V_{hv} = 200 V, load = 2 kW

Result: turn-on current of Q7 is reduced from **45.2 A to -3.1 A**

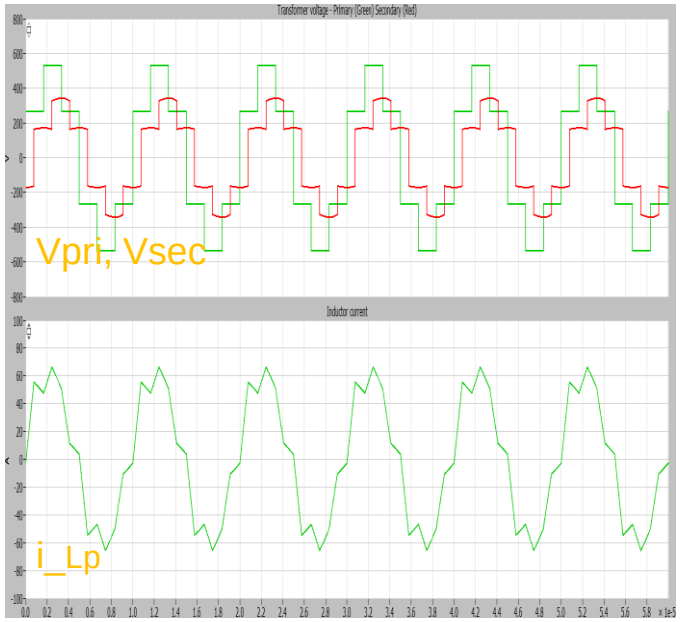
Modulation scheme 2: SPS + complementary PWM
(D0, D3=D4, when $V_{bus} < n * V_{hv}$)

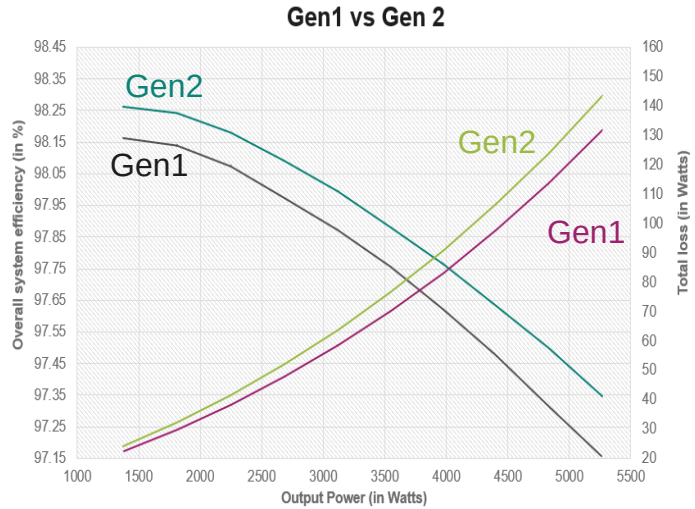




at V_{bus} = 900 V, V_{hv} = 900 V, load = 1 kW

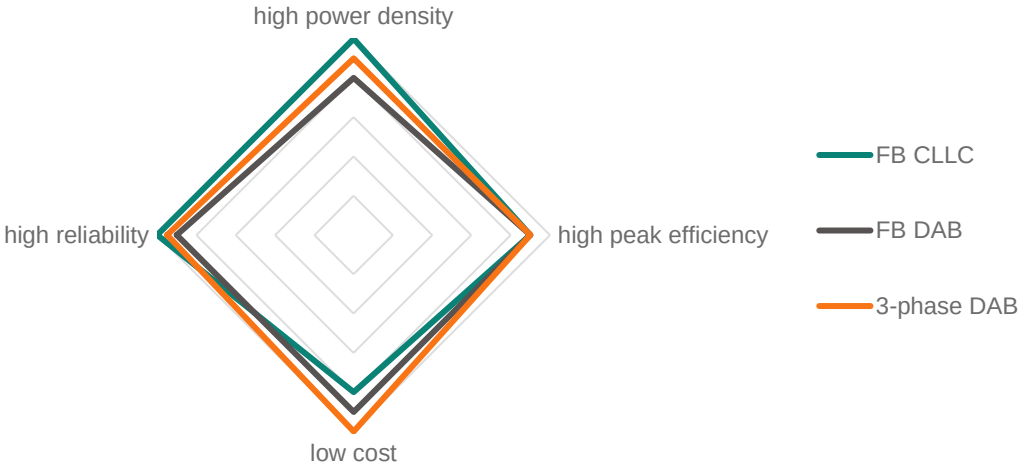
Result: turn-on current of Q1 is reduced from **24.7 A to 7.2 A**





Summary of CLLC and full bridge / 3-phase DAB:

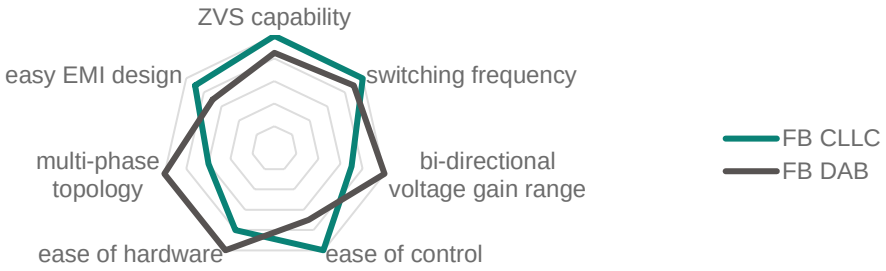
Top level assessment



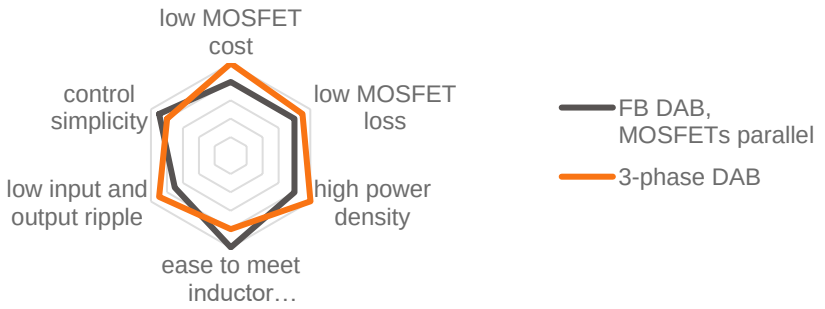
Main conclusions:

1. CLLC is the best choice, if high switching frequency, high power density and good EMI performance need to come together, and a narrow output voltage range is acceptable.
2. The key advantage of DAB for the use case of DC EV charging is its combination of wide output voltage range with a decent efficiency in both directions, and lower cost.
3. 3-phase DAB comes with the lowest semiconductor and passive component costs, but needs special care on the control concept

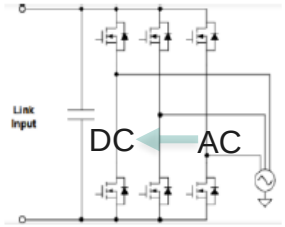
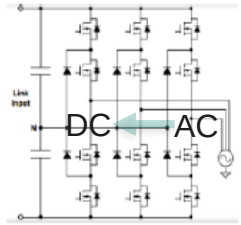
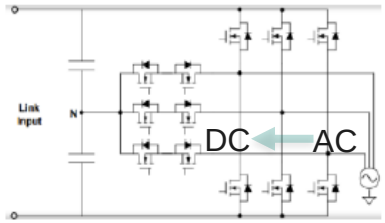
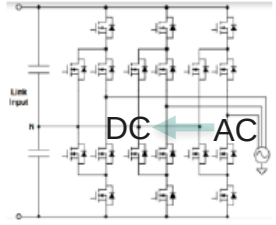
Full-bridge CLLC versus full-bridge DAB



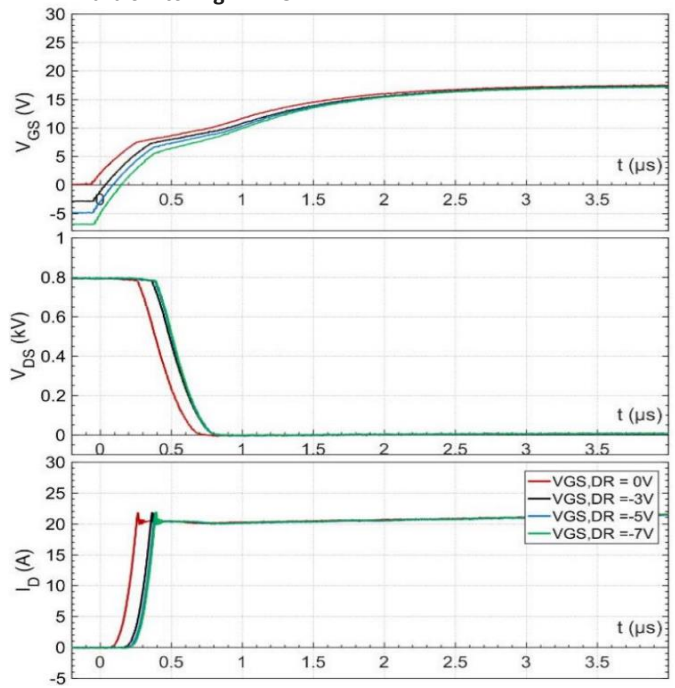
Full-bridge DAB versus 3-phase DAB

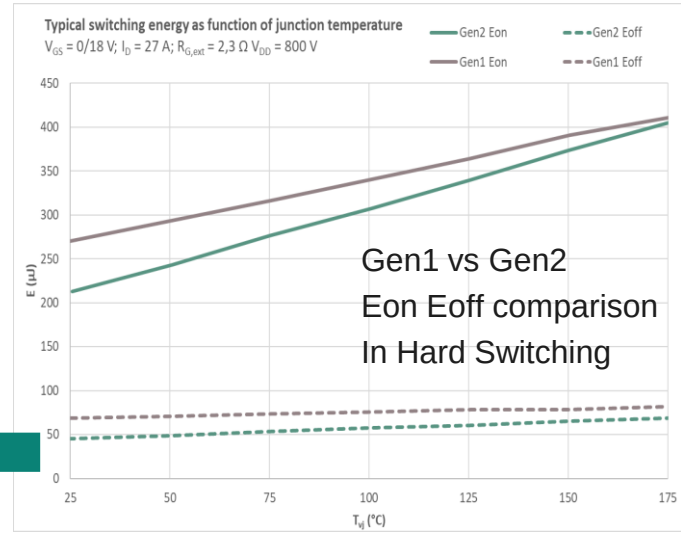


PFC Topology comparison and hard switching

Topology		Properties
Two level h-bridge		– Simple, well known architecture – Low component cost – Simple control structure – Losses are concentrated in few devices – Link voltage limited to component voltage rating
Three level NPC 1		– Stacks multiple switching devices to half the voltage blocking capability needed – Able to use lower voltage/cost devices – Neutral point clamp centers switching devices – Unequal component loss distribution – Increased conduction loss – More complex control structure
Three level NPC 2 / TNPC		– Reduced switching device count – Lower conduction loss – Simplified driver bias supply vs NPC1 & ANPC – Simplified control structure vs NPC 1 and ANPC – Primary switches still experience full DC link voltage (blocking)
Three level ANPC		– Clamping diode replaced with active device – Similar benefits of NPC 1 – More complex control structure – Similar losses to NPC 1 but balanced across devices – Increased conduction loss

- RG = 10 Ω, VDC = 800 V, ID = 20 A, T = 25°C
- Hard switching in PFC





Hard switching in PFC topology, switching performance Improvement is more important for system efficiency up

Actual Switching waveform

Gen1 and Gen2

Actual switching waveform Comparision


Infineon