Infineon’s innovative top-side cooled package solution

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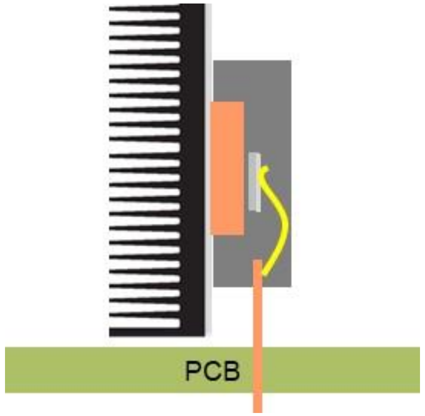
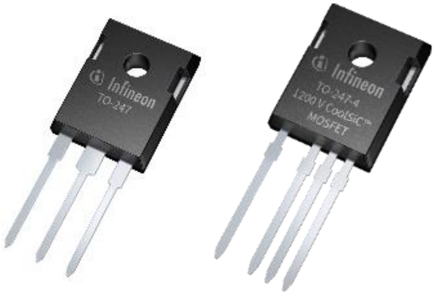
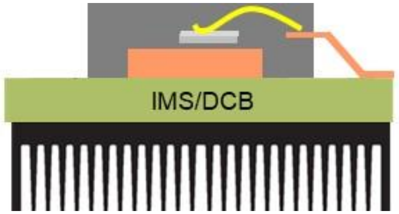
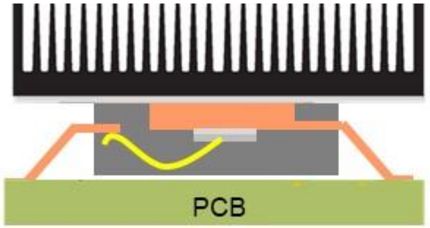
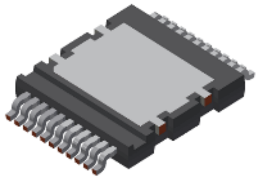
Package evolution which enables high volume assembly and PCB design improvement at expensive assembly location











THD – Through Hole Device

- Robust thermal performance
- Manual handling
- Low pin count, improved with 4-pin variant

SMD Bottom-side cooling

- Medium thermal performance
- Fully automatic handling
- High pin count

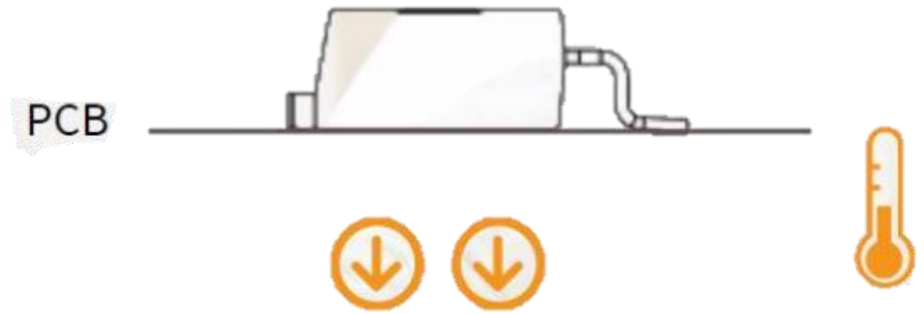
SMD top-side cooling

- **Optimal** thermal performance
- **Fully automatic** handling
- **High** pin count

Top-side cooling (TSC) with novel high-voltage packages

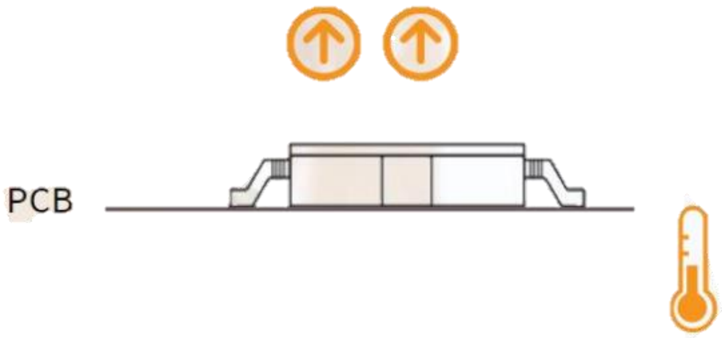
Bottom-side cooling

High voltage switch cannot be driven at higher power levels than PCB's thermal limit



Top-side cooling

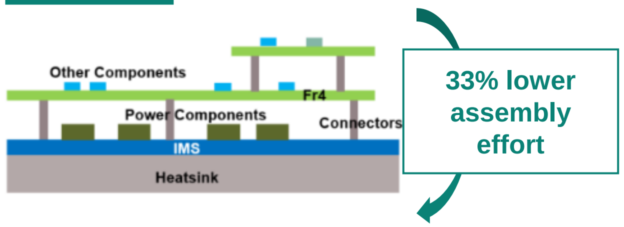
High voltage switch cannot be driven at higher power levels than PCB's thermal limit



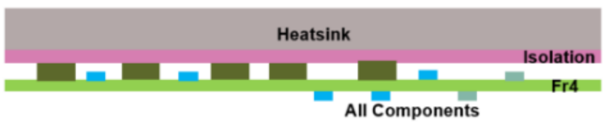
Advantages of Infineon SMD top-side cooling

Power density

BSC

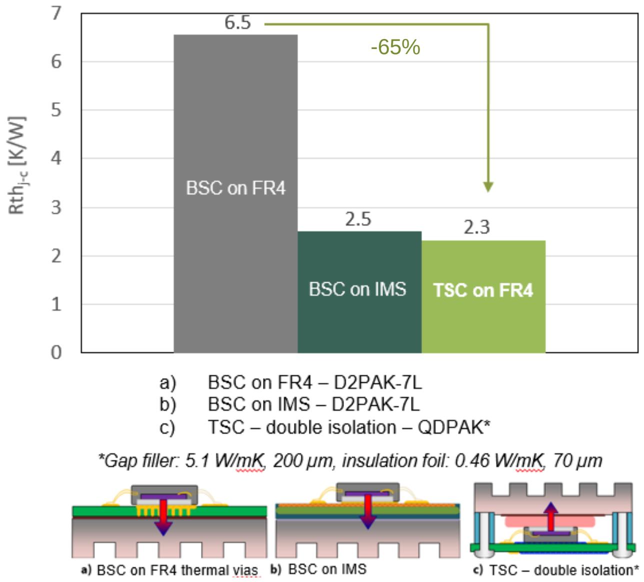


TSC



- Complexity reduction
- Simplified assembly
- IMS board eliminated

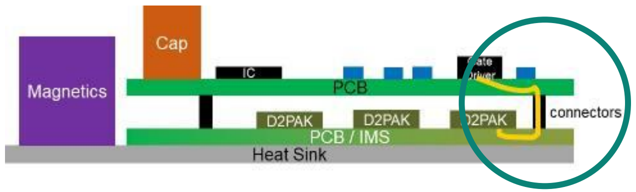
Thermal performance



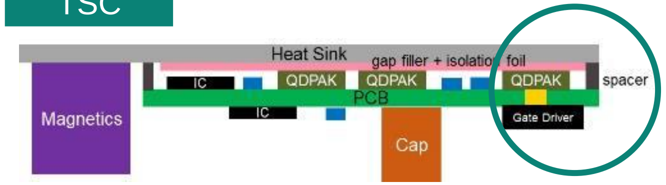
- 65% lower thermal resistance
- Overcomes PCB thermal limits
- Allows for cost optimized thermal designs

Electrical design

BSC

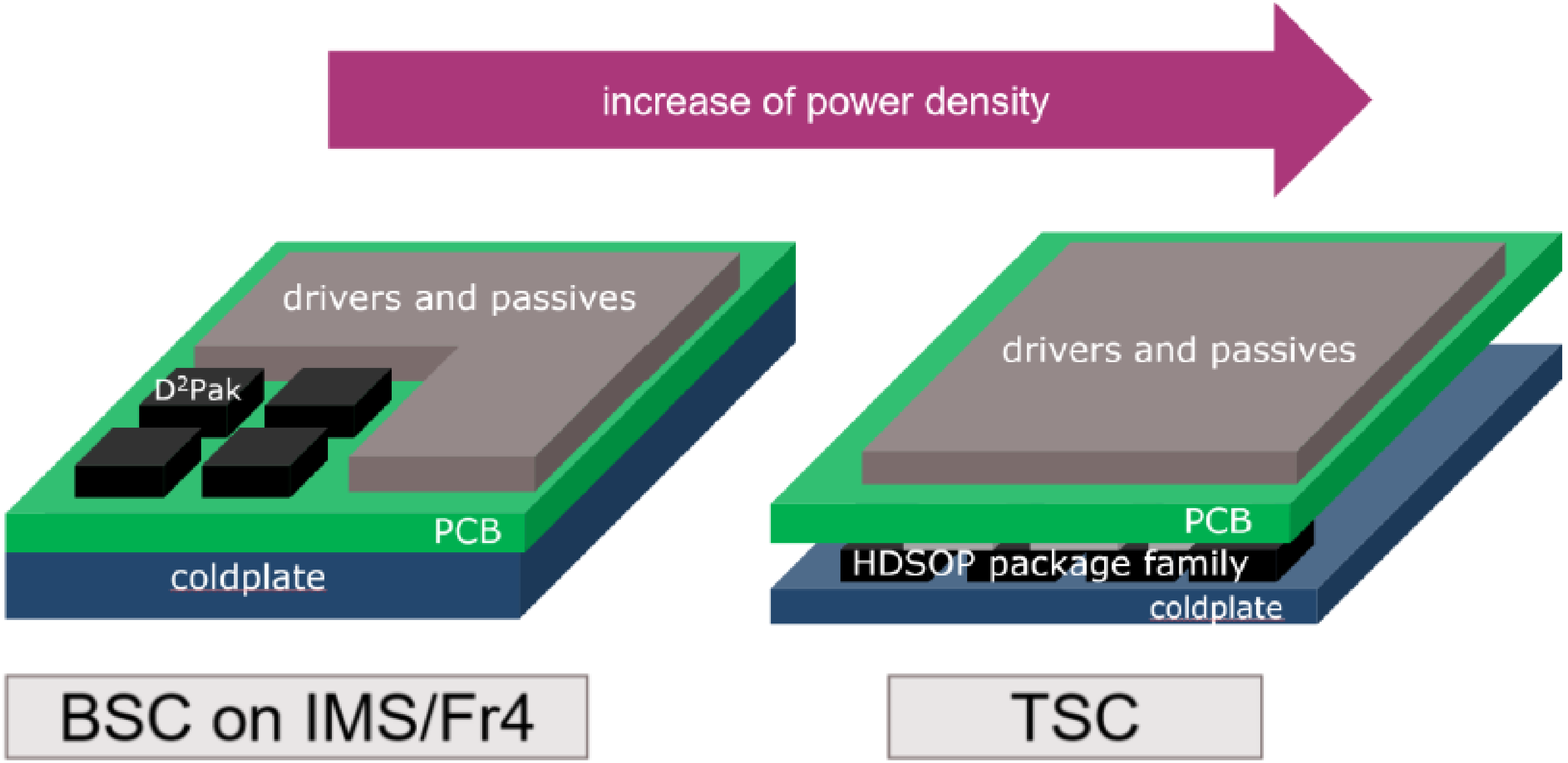


TSC



- Double sided PCB assembly
- Flexible PCB design
- Lower stray inductance
- Improved gate control

Improved power density of system



Top-side cooling enables faster assembly at lower system cost

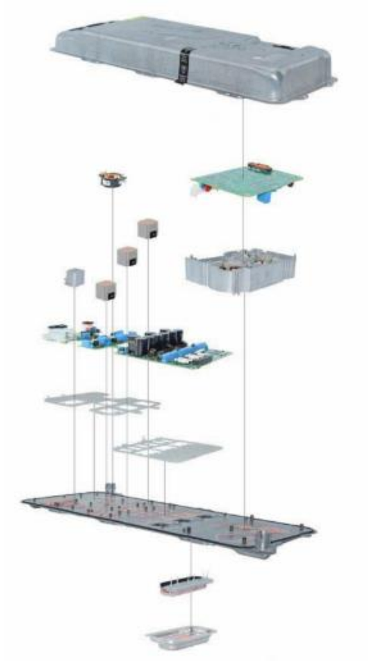
Simplified assembly

-76%

Number of connectors

PCB: FR4

- **No stacking** of different boards needed
- One big FR4 PCB:
  - all power components
  - and IC/driver/magnetics



System cost optimization

-33%

Assembly costs

-18%

FR4 PCB cost

Faster and highly automated manufacturing paired with lower assembly cost are key benefits

* Assembly analysis based on A2MAC comparison of traditional vs top side cooling design

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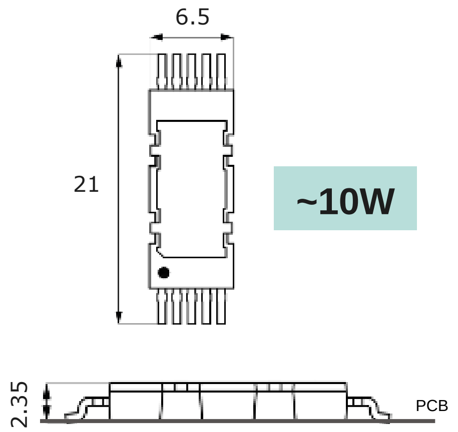
Infineon's top side cooling solution

DDPAK

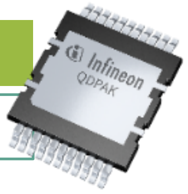
JEDEC registered

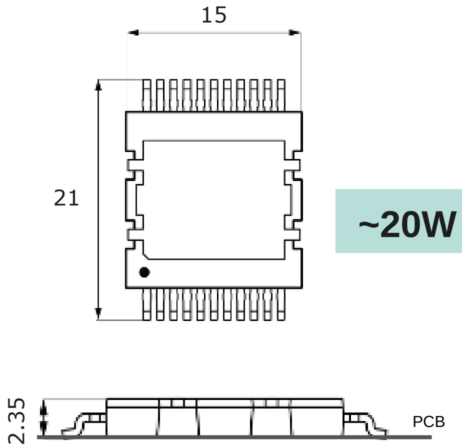


~10W

QDPAK

JEDEC registered

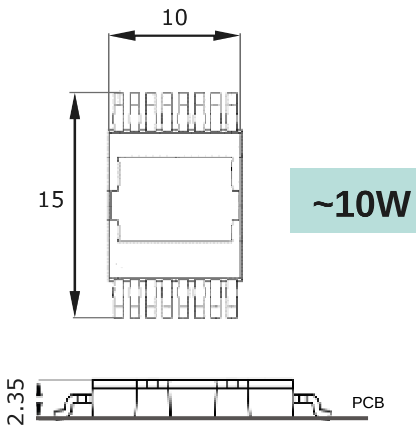




~20W

TOLT

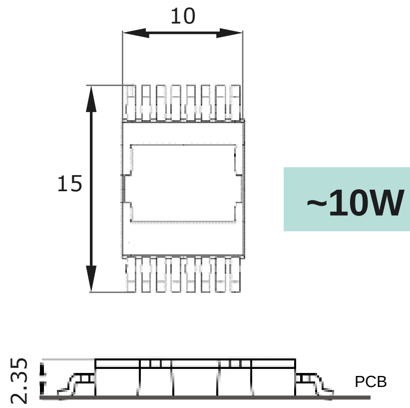
JEDEC registered



~10W

TOLT HV

JEDEC registration ongoing



~10W

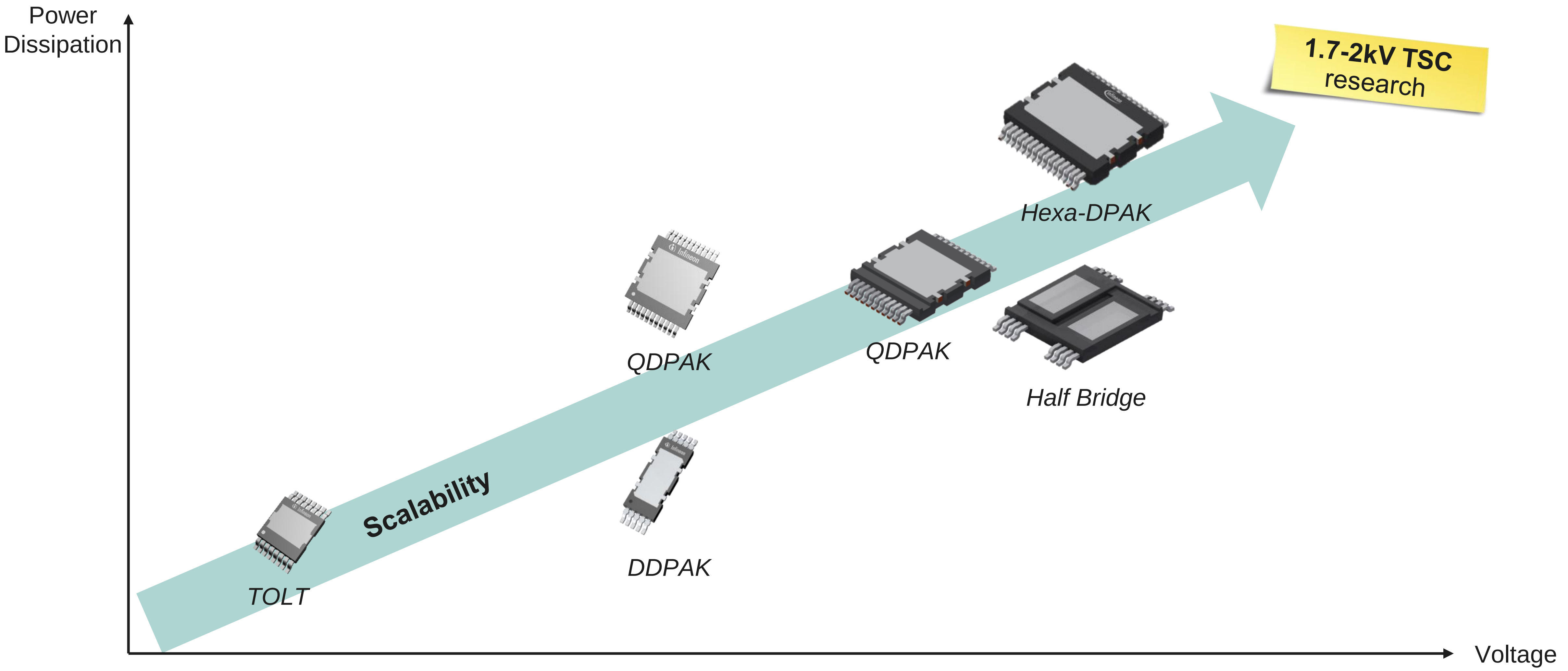
Note: All dimension in millimeters

Top-side cooling (TSC) status and next steps

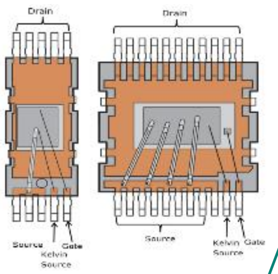
- Infineon Technologies is fully convinced about TSC. We extend JEDEC registrations:
  - High voltage TOLT registration ongoing
- Further package versions to come
- Multisourcing activity started via subcon

* Within the framework of competition and antitrust law

The QDPAK package is part of a scalable, future proof package concept to address various applications and customer needs



Power-density, opti-cooling and system-cost down DDPAK/QDPAK: thermal performance



QDPAK TSC

Increased power density: better use of PCB space.
Usage of kelvin source connection and reduced parasitic source inductance

Improved stability for extreme high current handling and **system lifetime** due to reduced temperature

PCB layout flexibility: enabling for new assembly areas. IMS board eliminated, single FR4 PCB used on both sides for all power components

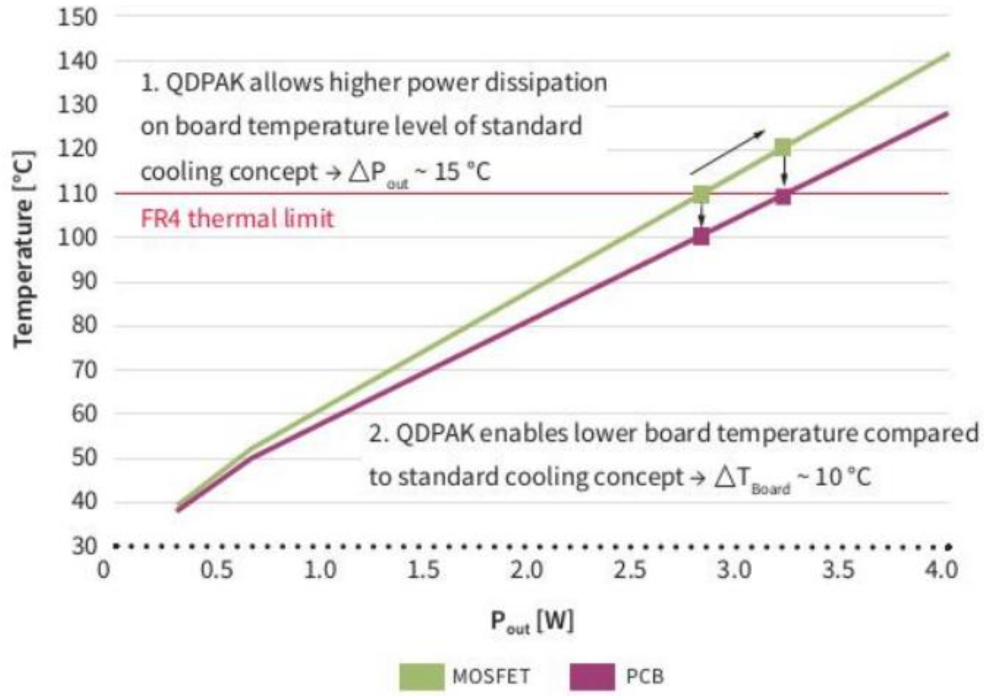
Improved thermal performance: connecting the top-side of the package to the heatsink allows higher chip temperatures. Decoupling of device and PCB thermal paths for optimized cooling

Manufacturability advantage: enabling high level of automation.
Reduction of assembly cost in a typical OBC of 33%

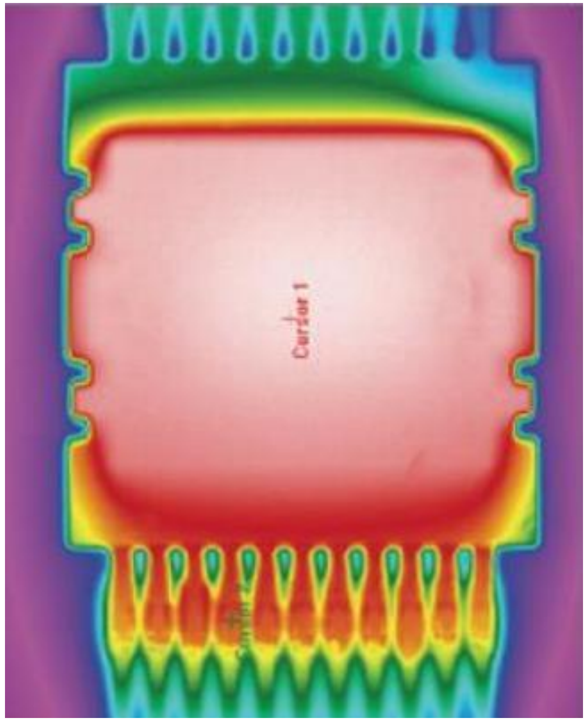
Minimized conduction and switching losses due to optimized package and bigger chip implementations possible

Power-density, opti-cooling and system-cost down QDPAK: cooling concept without cooling-system

Top-side temperature vs. PCB temperature of a QDPAK



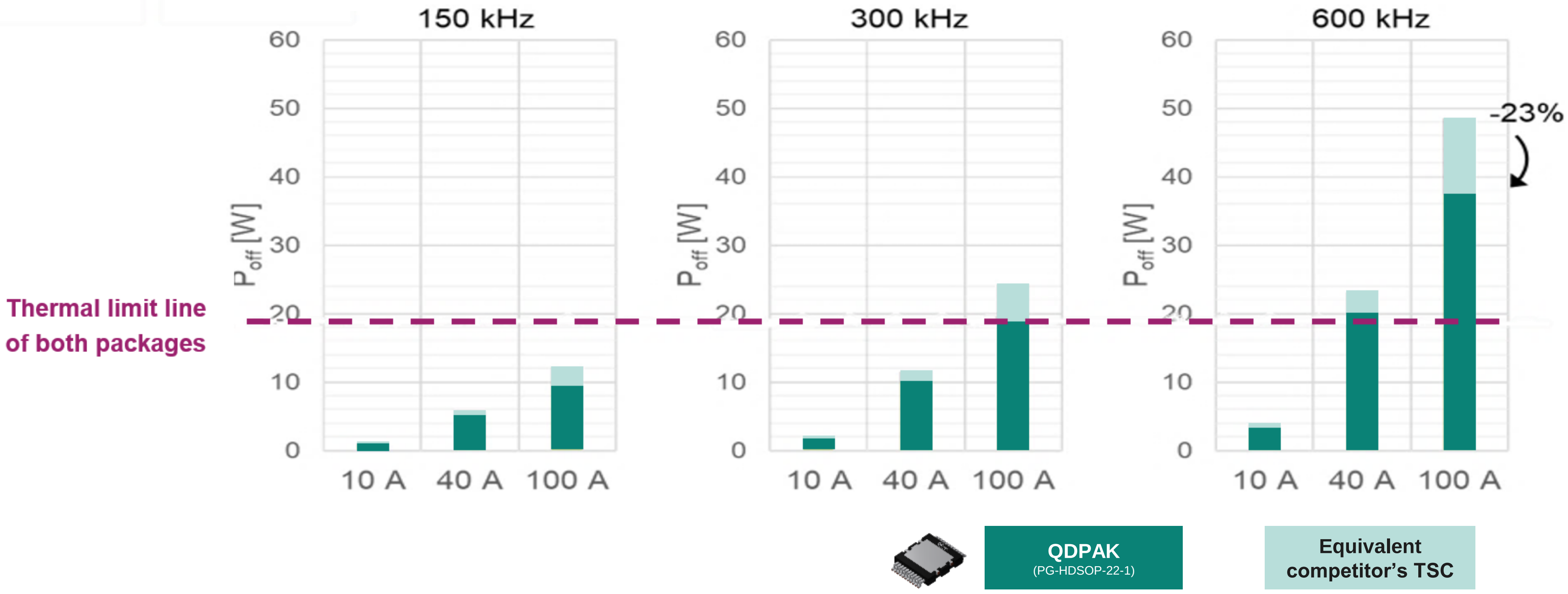
Heat distribution (top-side view)



This allows to:

- **Increase the power dissipation** by roughly 15 to 20% at the given PCB temperature
- **Improve the system lifetime** at lower board temperature ~10°C

QDPAK TSC shows less stray inductance than equivalent devices



Data-based on simulation in HF LLC under ZVS operation with 20 nH loop inductance, 6 nH gate inductance and different package parasitics

QDPAK:

- Offers up to 23% lower switching losses than competitor’s TSC in LLC converter
- Allows higher system output power

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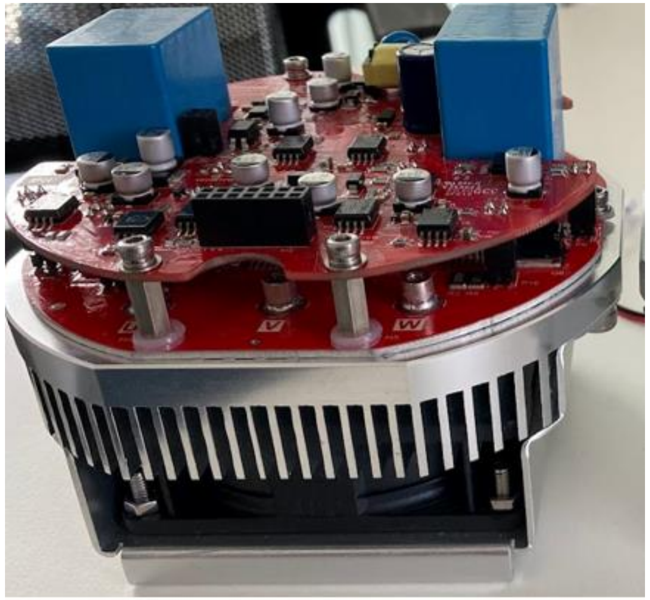
Significant production cost reduction with simplified design
1.2 kV SiC Servo Motor Drive Demonstrator

Standard cooling assembly

Stack: FR4 + IMS + 

- IMS board used for power components
- FR4 PCB used for IC/driver/magnetics components



Top-side cooling assembly

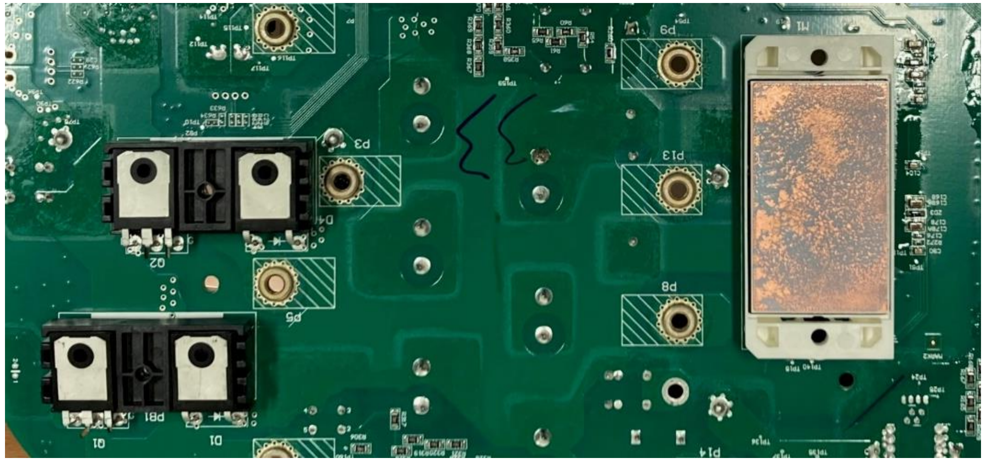
Stack: FR4 + 

IMS board eliminated

- Single FR4 PCB used on both sides for **all** power components
- Reduced stray inductance

- 65% Rth

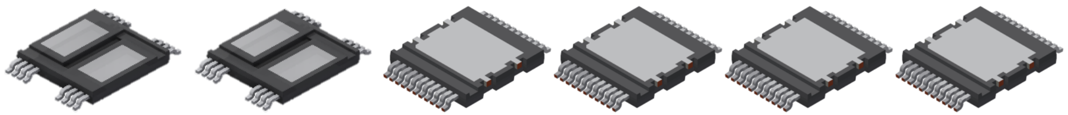
Example how to simplify Hybrid Solar inverter



- Booster
  - 2 IGBTs, 2 diodes in TO247
  - Requires extra bending* and manual* assembly/soldering
  - Plastic part used to enable heatsink connection*
- Inverter !Underutilized Module Package at lower power*
  - Modul with 4 IGBTs
  - Height is 12mm*
  - Manual* soldering or Pressfit assembly

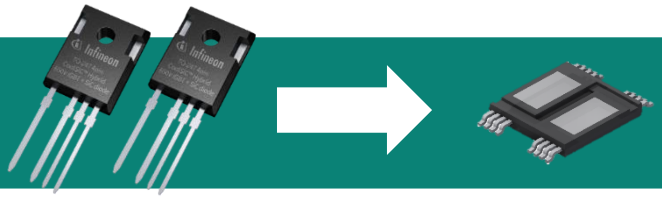
* waste

Lean design



- Booster
  - 2 QDPAK Boost with SiC to enable higher switching frequency
  - Automatised SMT assembly
  - Eliminated Plastic parts
- Inverter
  - 4 QDPAK H7 IGBT or SiC
  - Automatized assembly
- **TIPP**: the same 2.3mm package profile height enables flat heatsink connection

Easy scaling up to 50kW with half of semiconductor devices



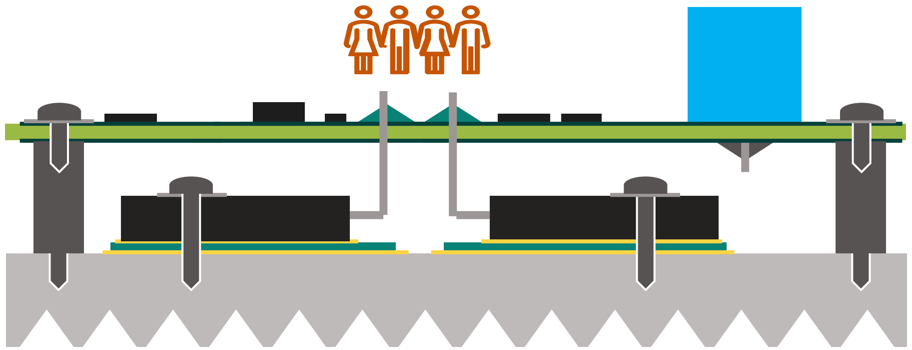
Smart Circuit Breaker with lowest assembly cost and most compact design – 1.2kV SiC Best-In-Class 4mΩ Demonstrator

Standard cooling assembly with 7mΩ

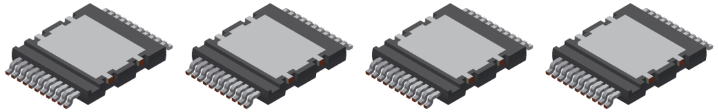
Stack: FR4 + 

- Manual lead bending*
- Manual soldering*
- Bulky design is conflicting with housing limitation*
- Heatsink and PCB connection required*
- Current density limitation

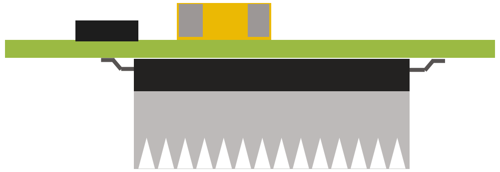
* waste

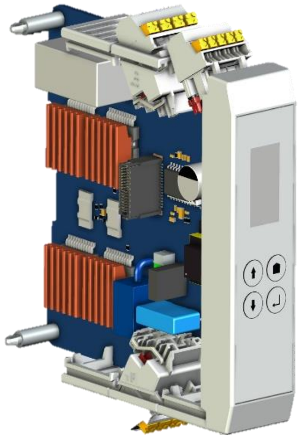


Top-side cooling assembly with BIC 4mΩ

Stack: FR4 + 

- Automatized SMT assembly
- Eliminated lead bending process
- Most compact design
- Direct heatsink soldering to package without isolation and can stay in the housing
- Z_{th} improvement
- Distributed current density into the PCB due high number of pin counts





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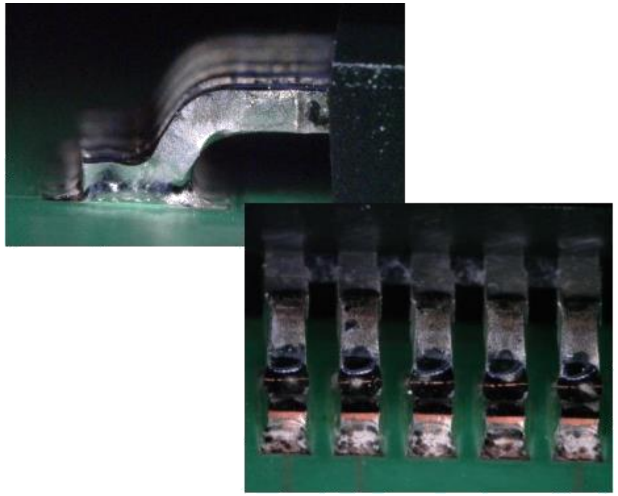
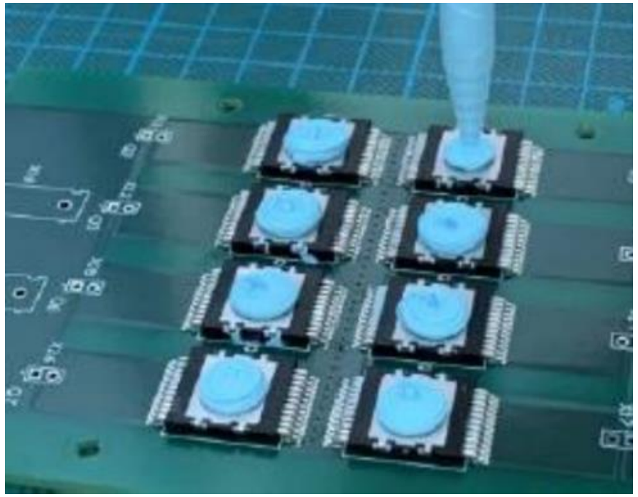
QDPAK heatsink assembly with gap filler

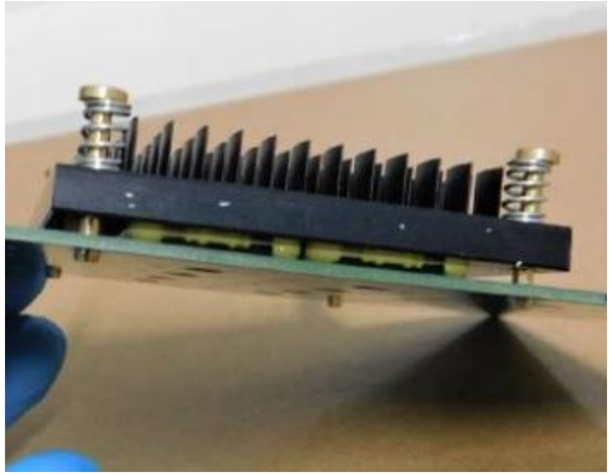
Reflow soldering of all SMD components → **Apply the gap filler** → **Mount the heatsink**



Package is for reflow soldering process only, wave soldering is not recommended
(possible shorts on leads)



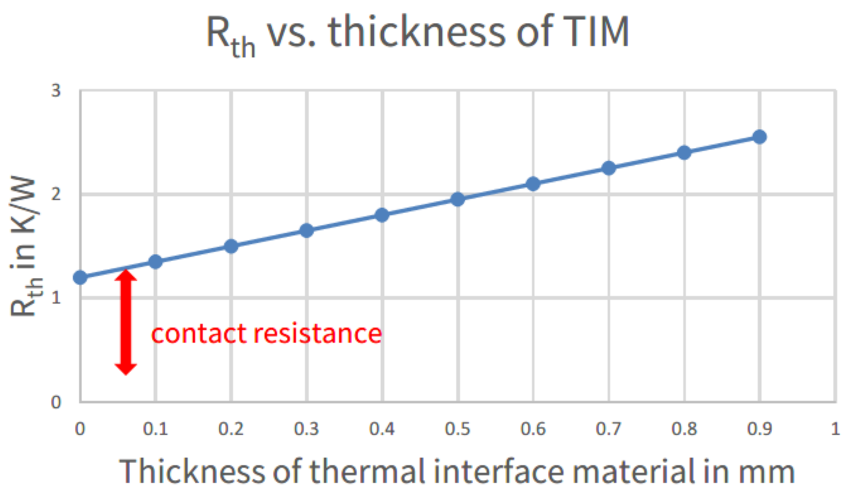
To achieve a good isolation a certain thickness of the gap filler or the usage of an additional isolation foil is required
(depends on PCBs thickness/stability, amount of components ….)



Several heatsink assembly methods are supported, this is just an example

Thermal interface materials

TIM	Consistency	Contact pressure	Comment
Gap filler pad	Solid (silicone or acrylic)	High	-. pre-cured silicone and ceramic powder materials -. high contact resistance -. do not conform well to their environment without significant force being applied
Liquid gap filler	Liquid paste that becomes solid after curing	No pressure needed	-. conforms very well to different geometries -. achieves excellent thermal performance -. often messy, but dispensation can be automated
Phase-change materials	Solid (at room temperature)	Low	-. Sticky material, changes from solid to half-liquid state at the specified temperature to fill air gaps -. good thermal performance -. can only compensate narrow mechanical tolerances (up to 100um)

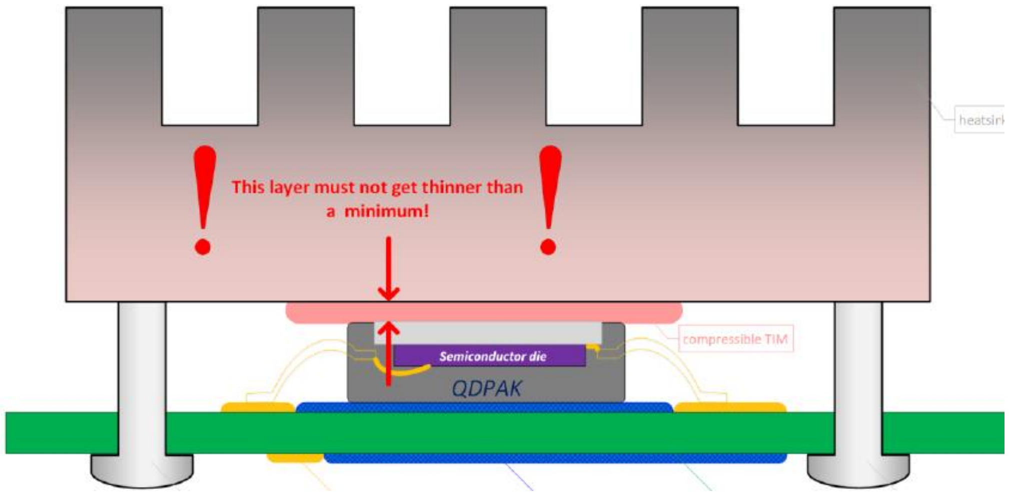


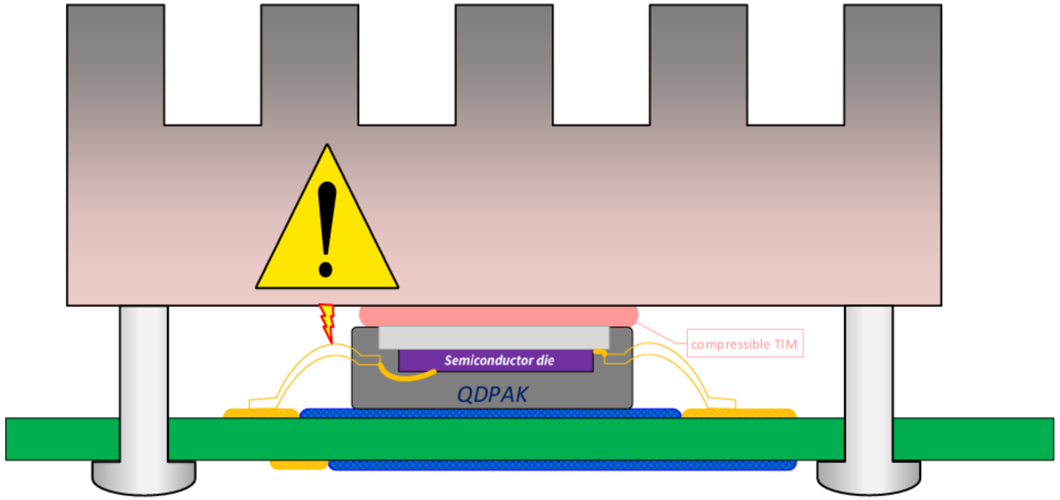
$$R_{th} = R_{contact} + R_{th\_material\_thickness}$$

$$R_{th\_material\_thickness} = \frac{TIM\_thickness}{TIM\_therm\_cond}$$

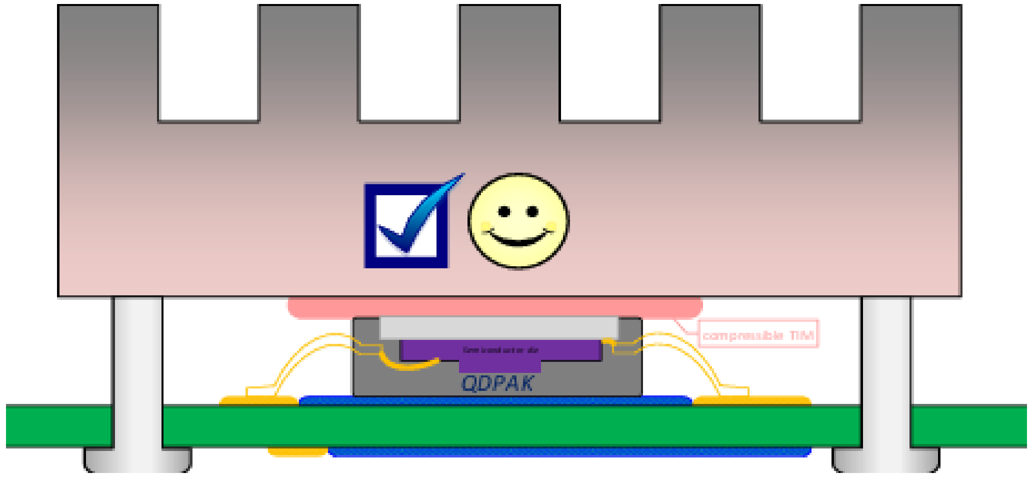
QDPAK heatsink assembly considering creepage and clearance optimization

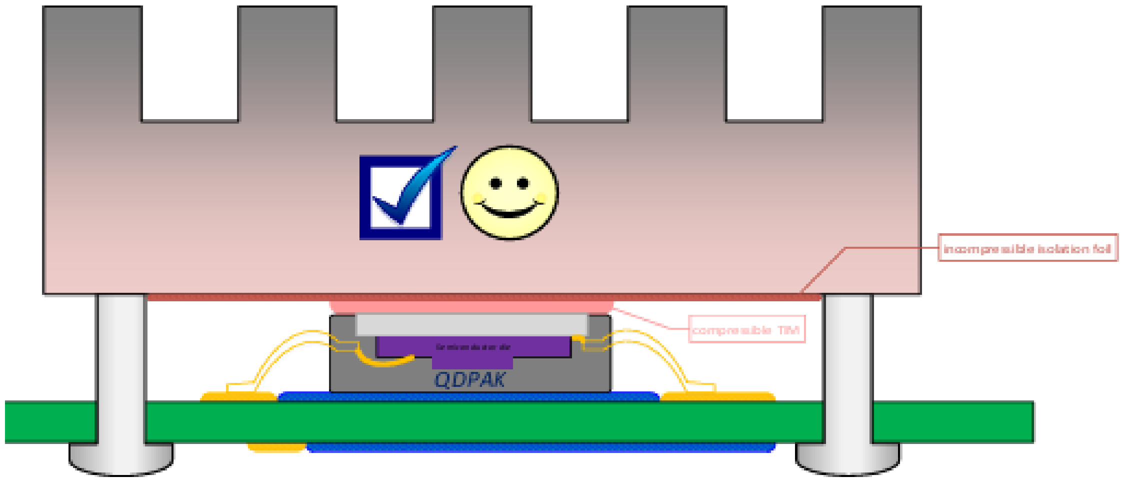
clearance and creepage violation





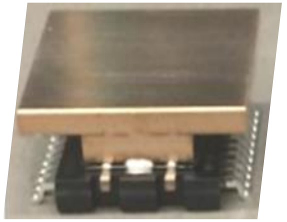
Recommendation





Mounting options for further top-side cooling

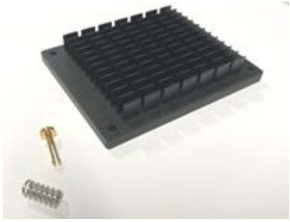
Heatsink on package with soldering



Solderable top side

- T-shaped heatsink recommended
- Additional isolation

Heatsink on PCB with push-pins



Push-pins

Heatsink

↓

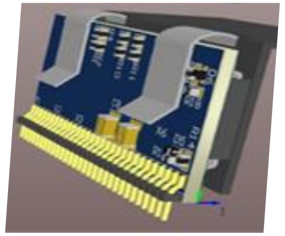
Packages

Heatsink on PCB with screws

Daughter card screwed down onto PCB

Homogeneous cooling ensured via correct foil thickness

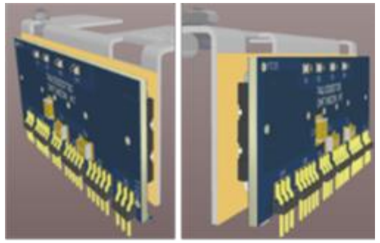
Heatsink on PCB with clips



Clips with special down force

- Number of components
- PCB thickness
- Component height
- TIM performance

Bond ply as isolation



Bond ply

Pressure-sensitive adhesive tape

↓

High bond strength

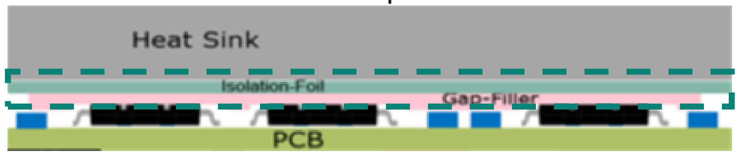
Isolation foil and gap filler

Height difference compensation

Isolation material

↓

Gap filler



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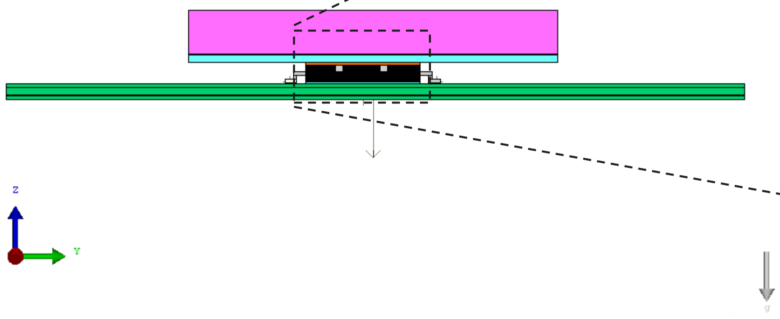
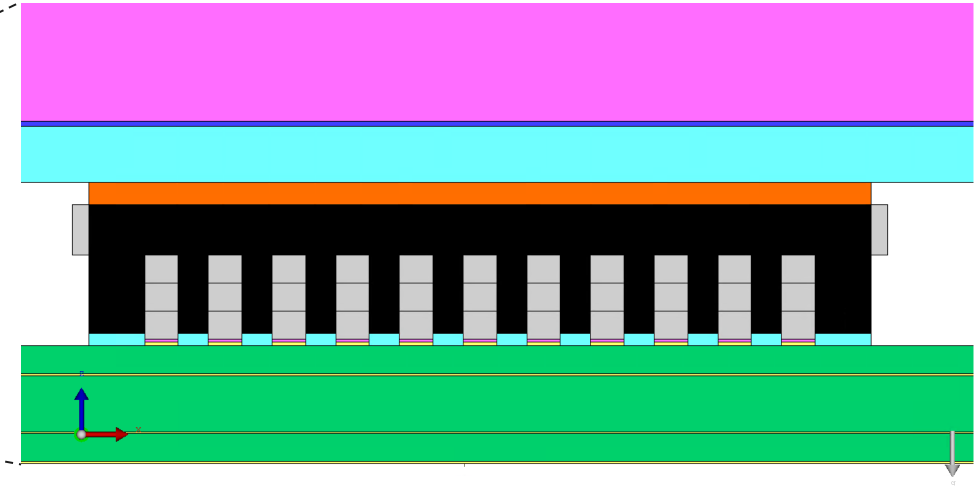
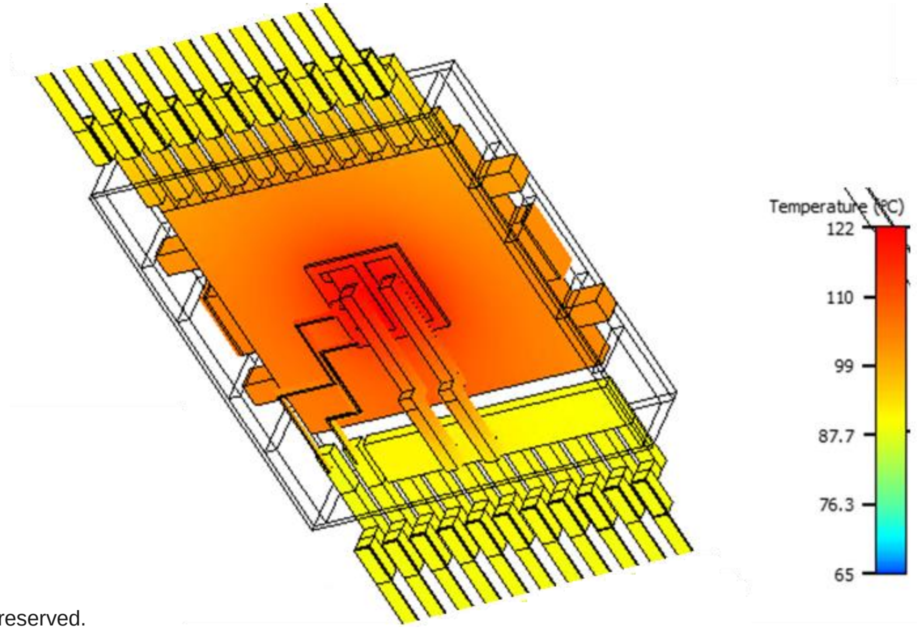
Thermal simulation & Tj estimation using Psi value

- – Mold Compound
- – Aluminum (heat sink)
- – Ceramic Plate
- – Thermal Grease
- – GapFiller
- – Lead Frame
- – FR4
- – Copper
- – Air Gap
- – Solder
- – Air







Estimated Tj = T_drainpin + ΔTj

ΔTj = Psi_j-drainpin * Power dissipation

Infineon