What are FOMs of SiC MOSFET

- How important they are

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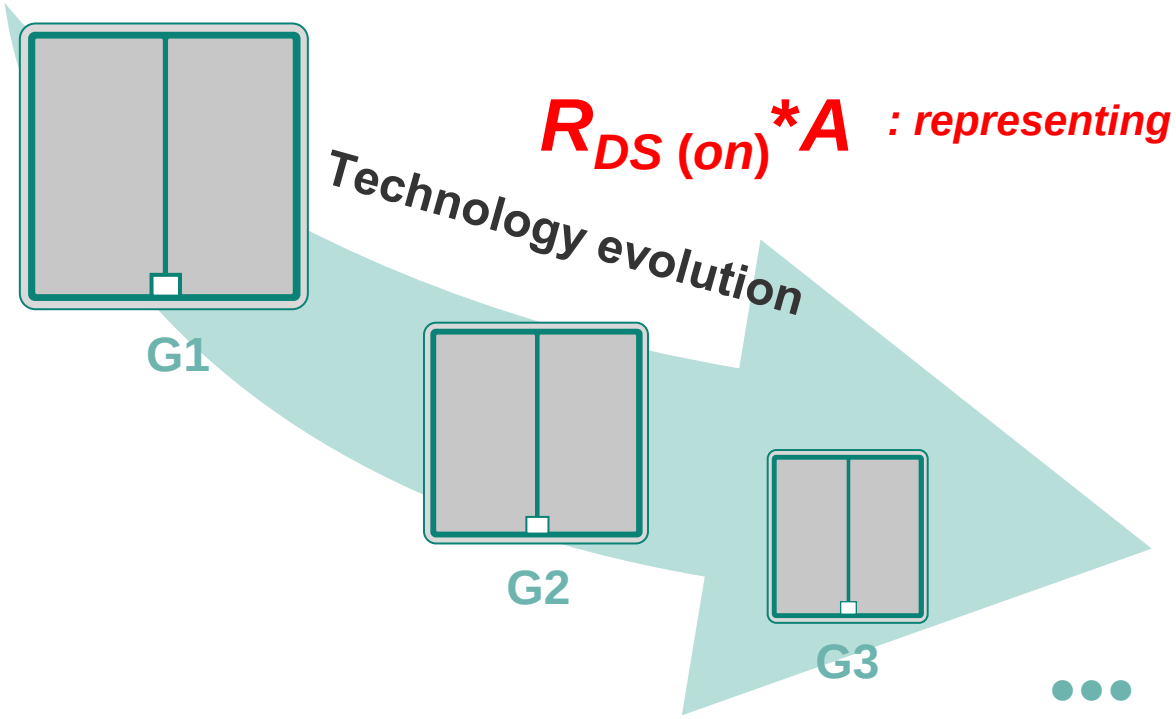
Goal of Presentation

- ✓ Understanding FOMs of SiC MOSFET
- ✓ How they are used in practical

FOM (figure of merit) of SiC MOSFETs

A numerical performance indicator of a device expressed by multiplied by $R_{DS(on)}$ and one or more parameters of device

- it will turn out to benefits
- The smaller the value, the better the performance

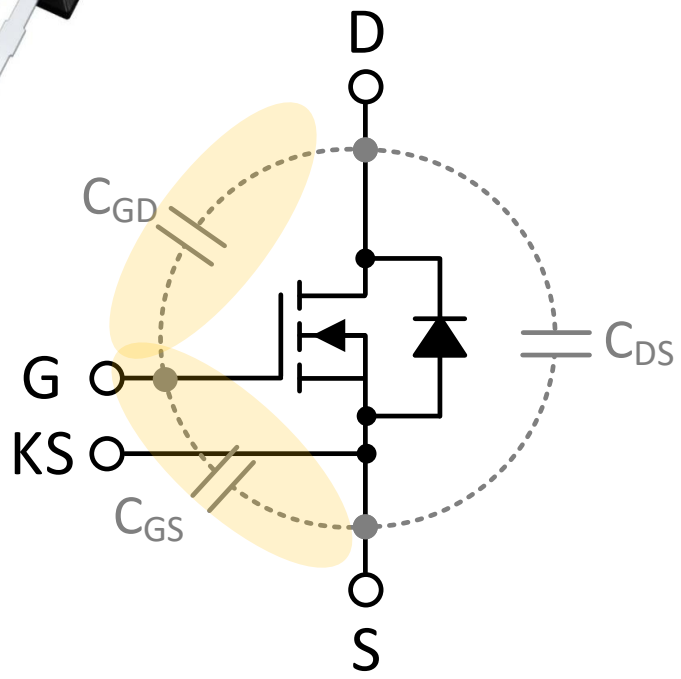


Is it really beneficial to system designers

?

Requires
Practically Meaningful of FOMs

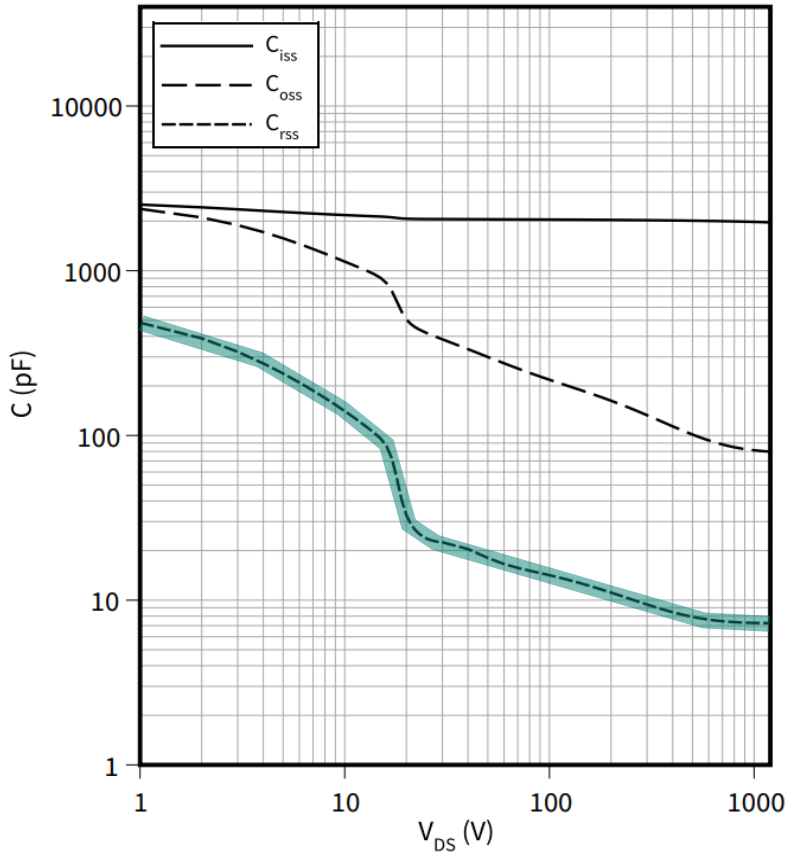
Input capacitance related



$C_{iss}=C_{GS}+C_{GD}$

$C_{rss}=C_{GD}$

$C_{oss}=C_{DS}+C_{DG}$



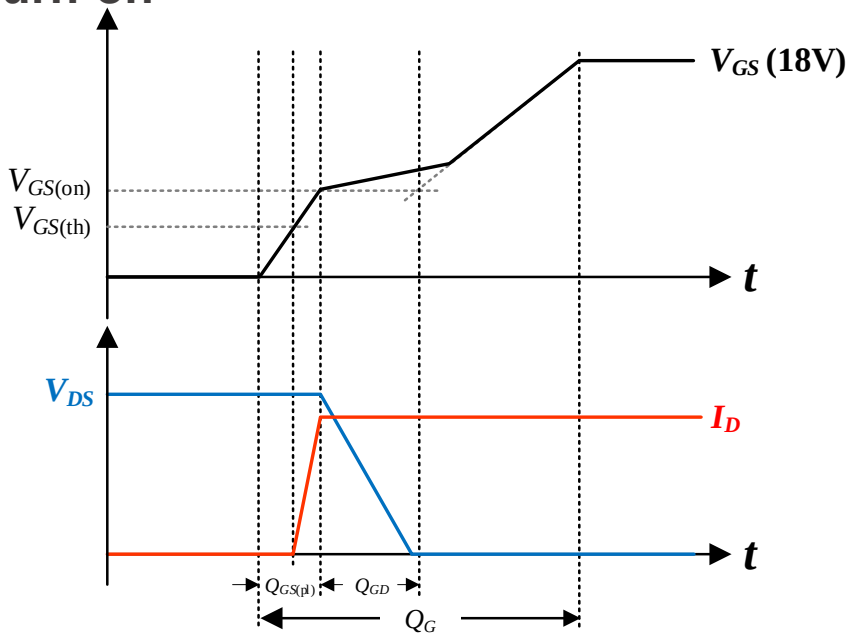
$R_{DS(on)}$*Q_{GD}

- Product of the drain-source on resistance $R_{DS(on)}$ and the gate charge Q_{GD}
- Can be good indicator to define from a conduction and switching performance perspective

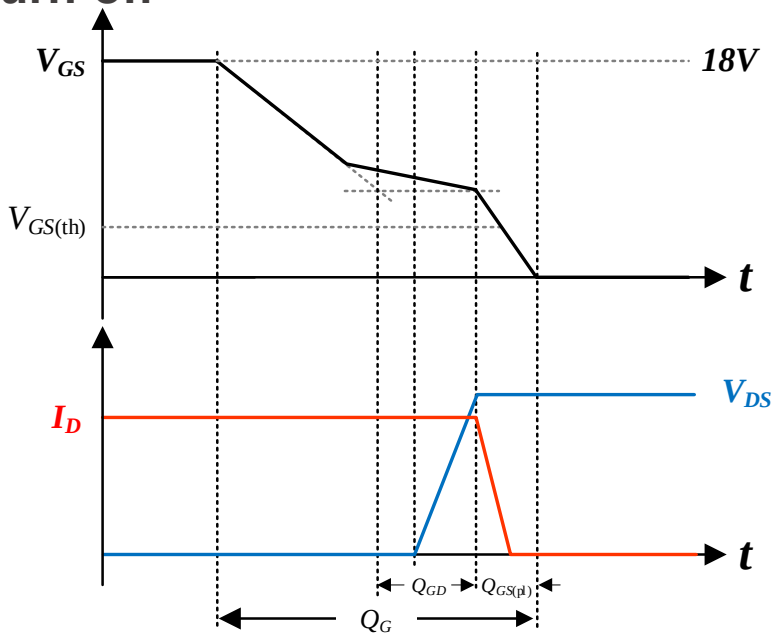
Example; IMBG120R026M2H

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Total gate charge	Q_G	V_{DD} = 800 V, I_D = 27.3 A, V_{GS} = -2/18 V, turn-on pulse		60		nC
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 27.3 A, V_{GS} = -2/18 V, turn-on pulse		12.9		nC
Gate-to-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 27.3 A, V_{GS} = -2/18 V, turn-on pulse		16.2		nC

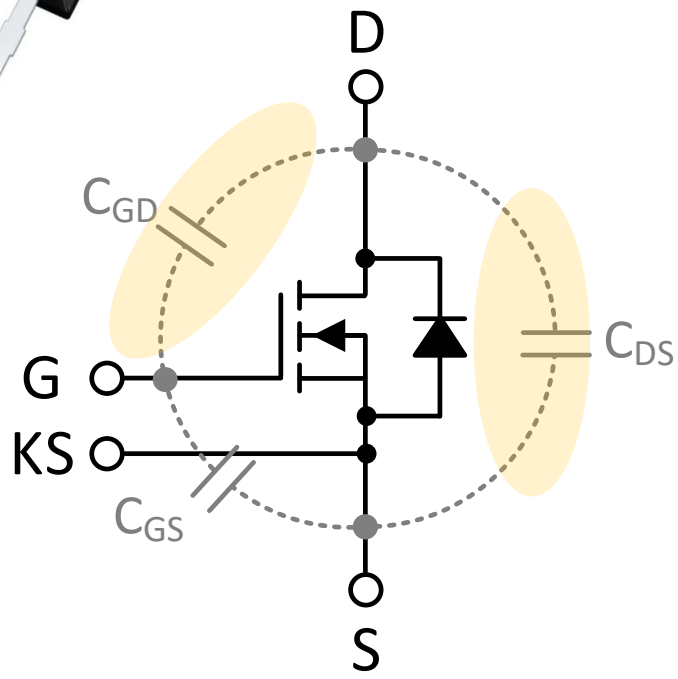
► Turn-on



► Turn-off



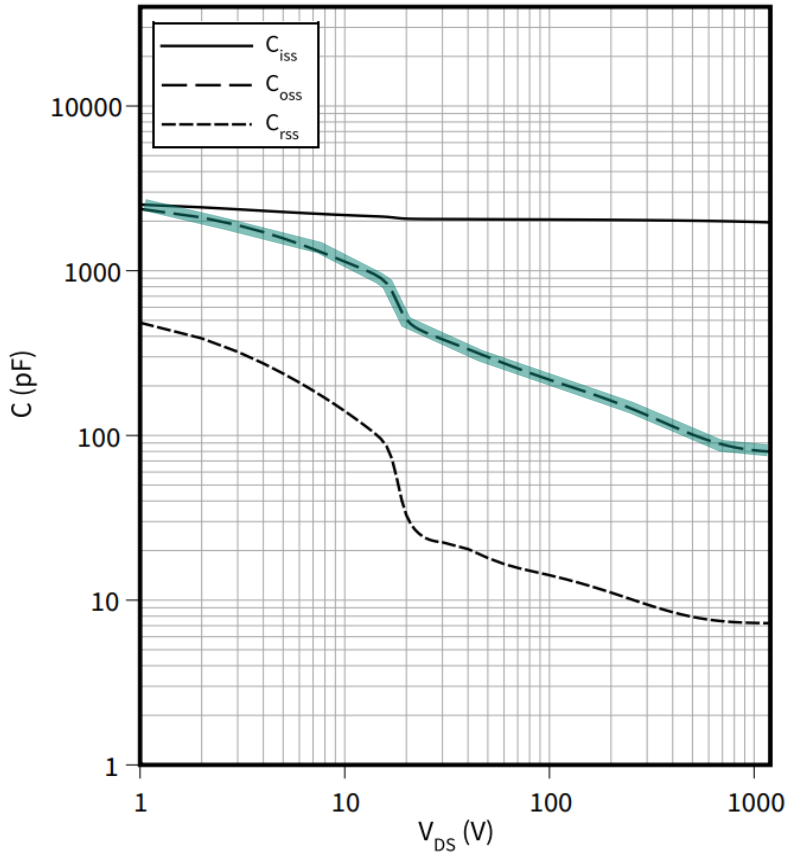
Output capacitance related



$C_{iss}=C_{GS}+C_{GD}$

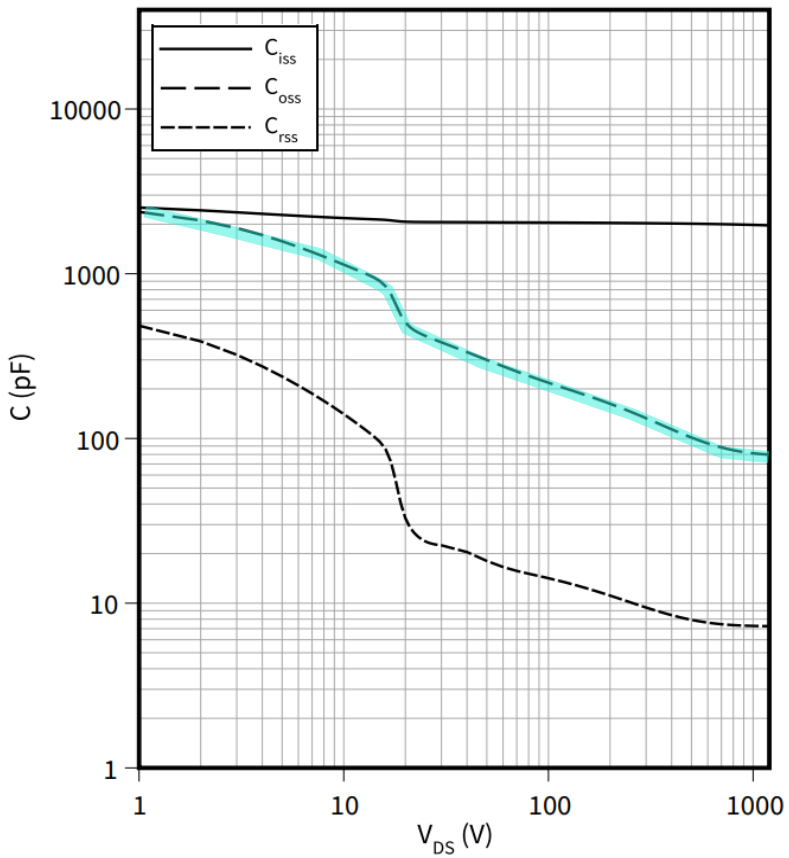
$C_{rss}=C_{GD}$

$C_{oss}=C_{DS}+C_{DG}$



C_{oss} (output capacitance) of SiC MOSFET

Example; IMBG120R026M2H



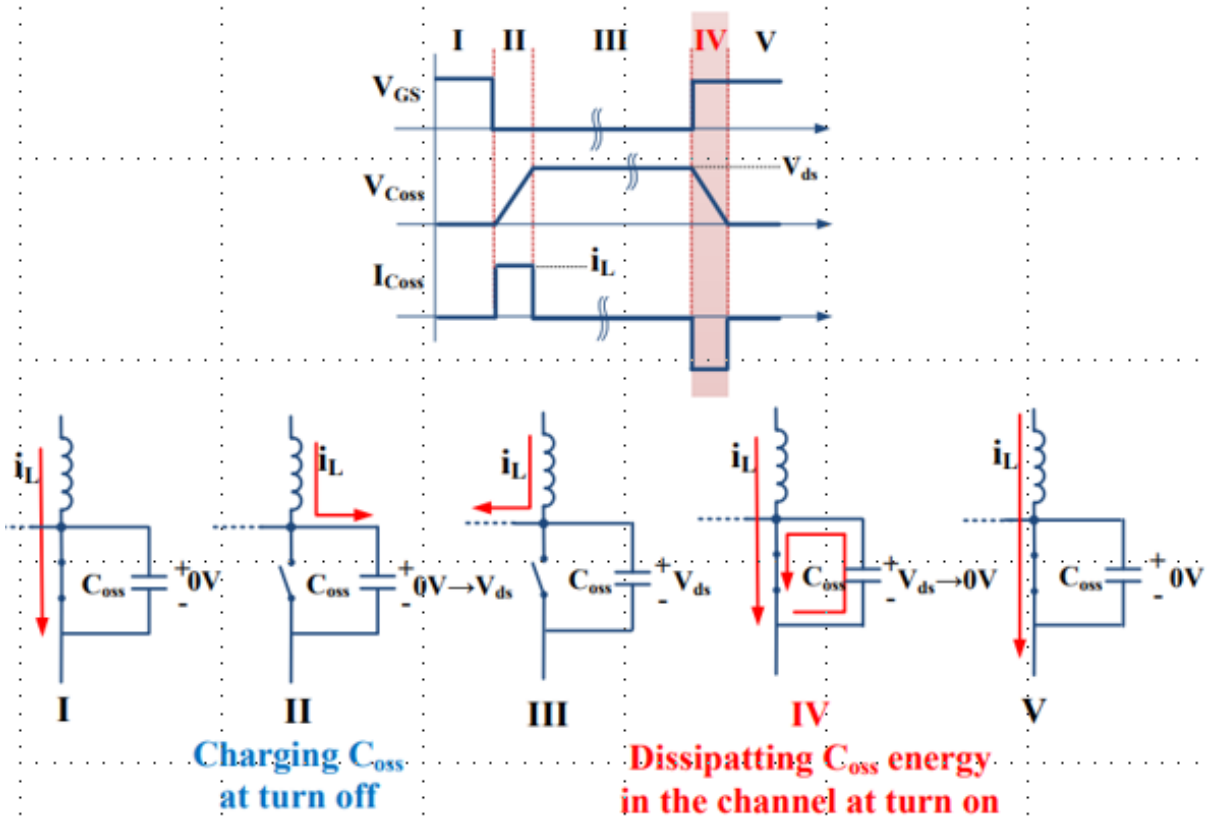
Typical capacitance as a function of drain-source voltage
C = f(VDS) f = 100 kHz, VGS = 0 V

- Not stable and proportional to Drain-source voltage
- C_{oss}, Q_{oss} and E_{oss} cannot correlate with each other unlike ordinary capacitor

$$E_{oss\_V_{DS}} \neq C_{oss@V_{DS}} V_{DS}^{\ 2} \neq C_{oss} Q_{oss@V_{DS}}$$

- One of crucial device parameter affecting system performance
- Need to consider each for different applications (hard switching or soft switching)

$R_{DS(on)}$*E_{OSS} or ($R_{DS(on)}$* $C_{o(er)}$)- Hard-switching related



- Indicating the intrinsic turn-on energy loss
- The smaller E_{OSS} value (in the equivalent $R_{DS(on)}$), the less switching energy loss induced
  - Regardless of the switching current
  - Proportional to the switching frequency
- In the worst case, $Tc(T_{vj})$ may significantly rise with no load condition at high switching frequency

$$E_{oss\_800V} = \int_0^{800} vC(v)dv = \boldsymbol{C_{o(er)}} 800^2$$

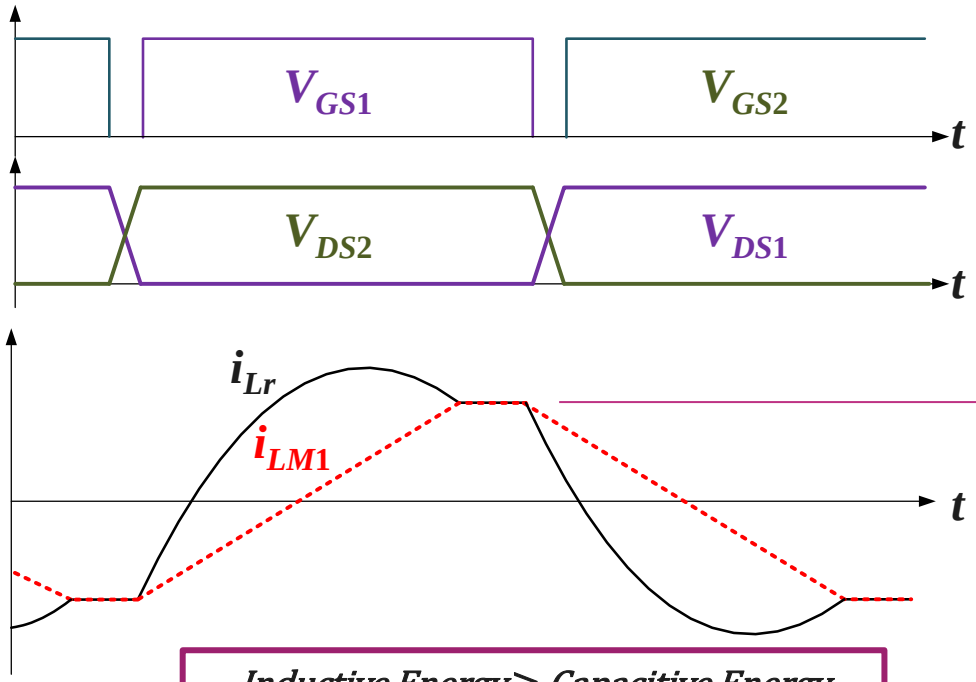
- It needs integration to get – hard for designer to know the value
- Infineon offers the value in datasheets from G2

Example; IMBG120R026M2H

C_{oss} stored energy	E_{oss}	V_{DD} = 800 V, V_{GS} = 0 V, f = 100 kHz, V_{AC} = 25 mV		36		µJ
Output charge	Q_{oss}	Calculated by $C_{oss}(f)V_{DS}$ @100 kHz		132.6		nC
Effective output capacitance, energy related	$C_{o(er)}$	V_{DD} = 0...800 V, V_{GS} = 0 V		112.5		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_C = constant, V_{DD} = 0...800 V, V_{GS} = 0 V		165.7		pF

$R_{DS(on)}$*E_{OSS} or $R_{DS(on)}$* $C_{o(er)}$ - Soft-switching related

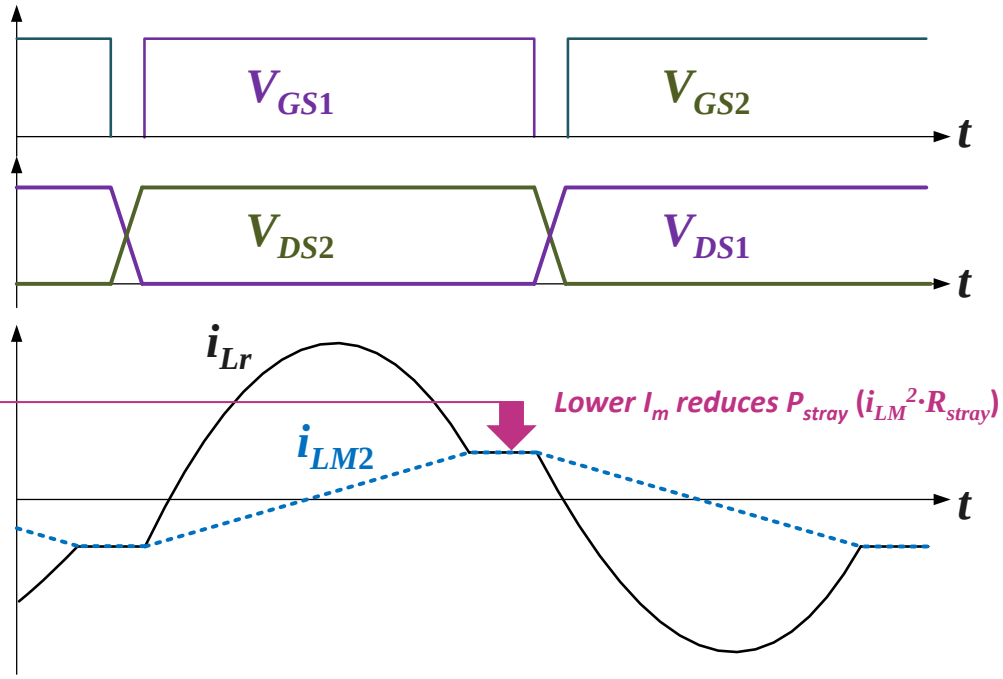
- LLC converter topology



Inductive Energy ≥ Capacitive Energy

$$\frac{1}{2}(L_m + L_r){I_{m\_pk}}^2 \geq \frac{1}{2}\left(2 \times C_{o(er)}\right){V_{DC}}^2$$

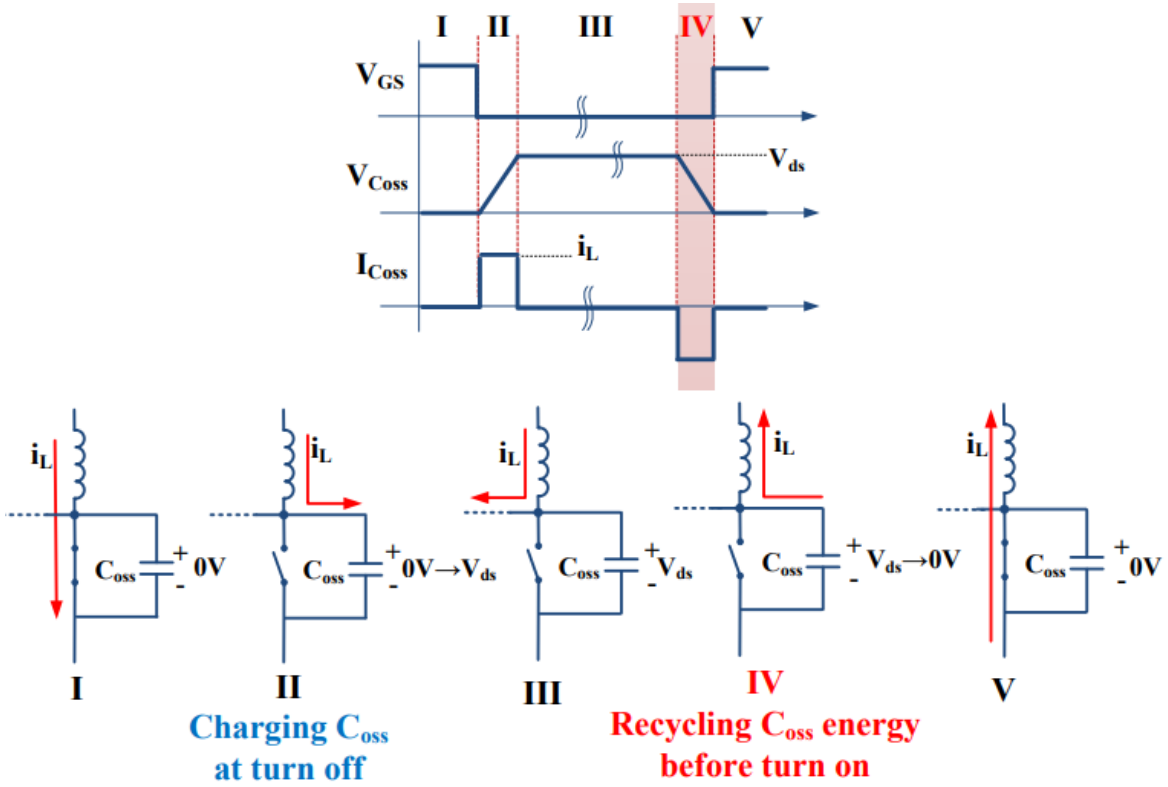
$$\frac{1}{2}(L_m + L_r){I_{m\_pk}}^2 \geq 2E_{oss}$$



Less $C_{o(er)}$ enables to lower magnetizing current for ZVS conditions

→ Improve system efficiency by minimizing losses by $i_{LM}^2 \cdot R_{stray}$

$R_{DS(on)}$*Q_{OSS} or ($R_{DS(on)}$* $C_{o(tr)}$) - Soft-switching related



$$Q_{oss\_800V} = \int_0^{800} C(v)dv = \boldsymbol{C_{o(tr)}} \times 800$$

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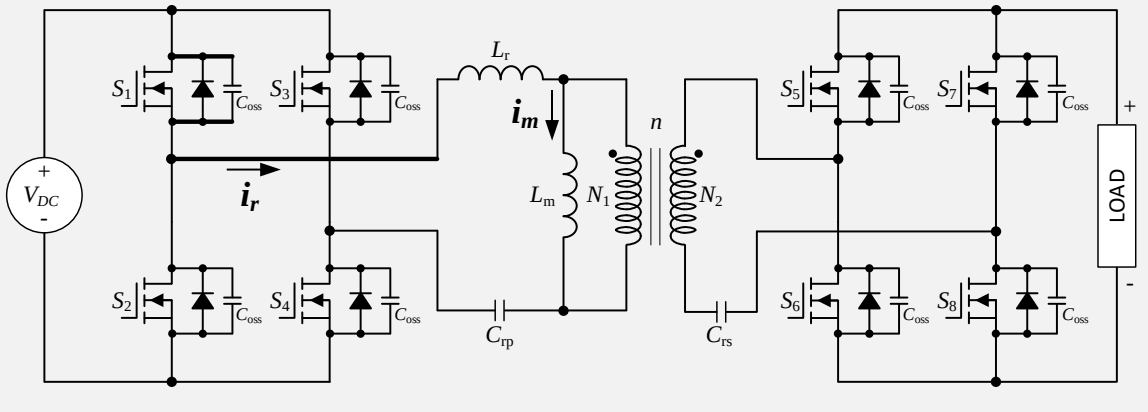
- Determining the deadtime to form ZVS (zero voltage switching) turn-on
- The smaller Q_{OSS} value (in the equivalent $R_{DS(on)}$) the less the deadtime
  - Minimizes the body diode conduction time
  - Enables higher switching frequency

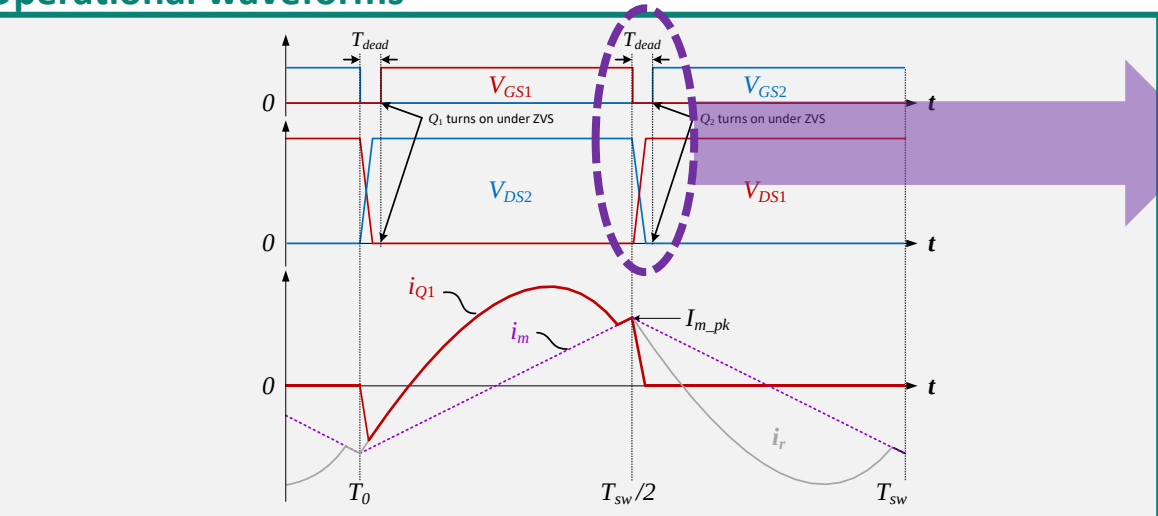
Where is Q_{oss}, $C_{o(tr)}$ considered

- Determining Dead-time LLC converter topology

CLLC converter topology



Operational waveforms



ZVS condition

$$\frac{1}{2}(L_m + L_r)I_{m\_pk}^2 \geq \frac{1}{2}\left(2 \times C_{o(tr)}\right)V_{DC}^2$$

$$I_{m\_pk} = \frac{V_{DC}T_{sw}}{4L_m}$$

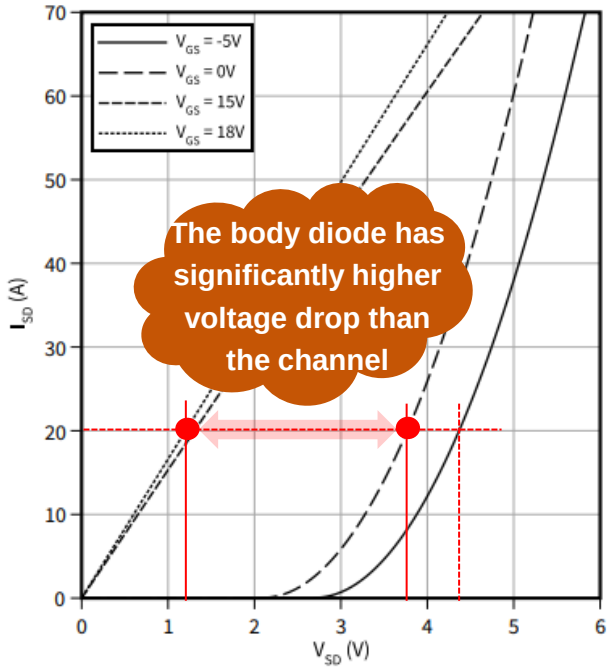
$$C_{o(tr)} \times f_{sw}$$

Example; IMBG120R026M2H

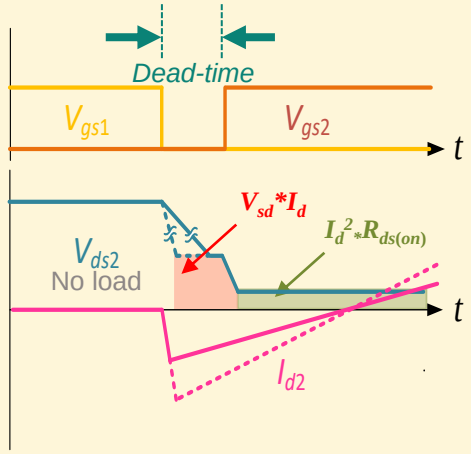
Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter

$I_{SD} = f(V_{SD})$

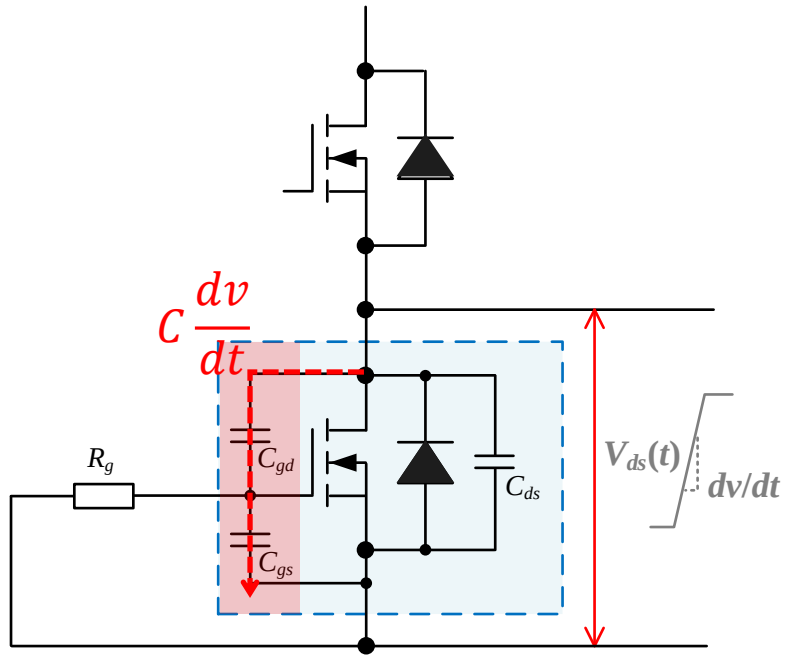
$T_{vj} = 175\ °C$, $t_p = 20\ \mu s$



Small Q_{oss} device



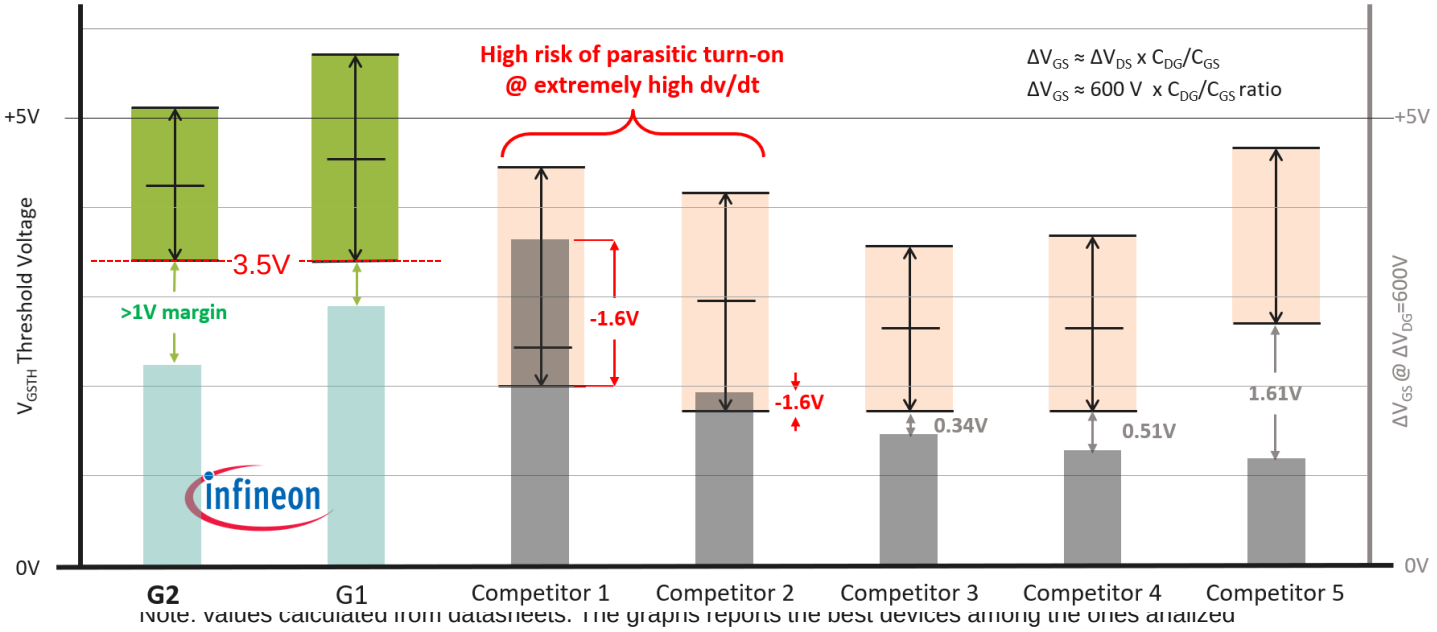
PTO (parasitic turn on) immunity: $1/V_{GS(th)}*Q_{gd}/Q_{gs}$



- PTO(parasitic turn on) event occurs when extreme dv/dt applies to the SiC MOSFET
- PTO increases the turn-on losses significantly and eventually can be potential device failure

$1/V_{GS(th)}*Q_{gd}/Q_{gs}$ is the FOM for determining the device safety from PTO

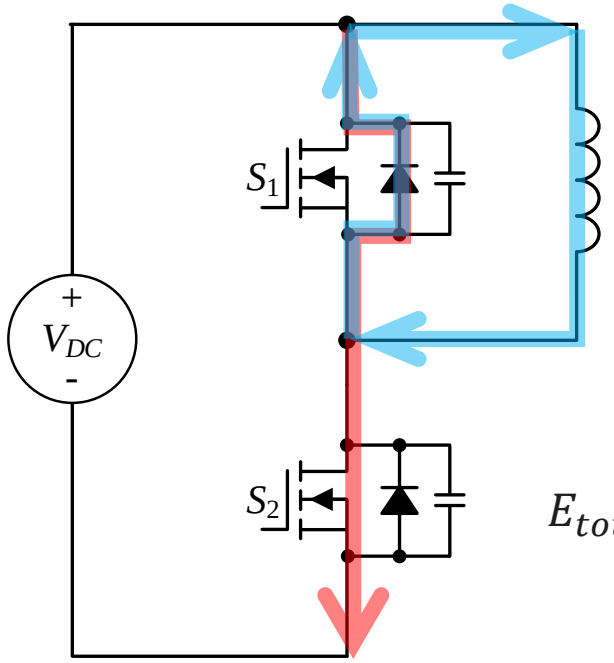
- The lower the **$1/V_{GS(th)}*Q_{gd}/Q_{gs}$** factor is, the less likely to have parasitic turn on
  → Enables to allow unipolar drive (0 V gate voltage turn off)



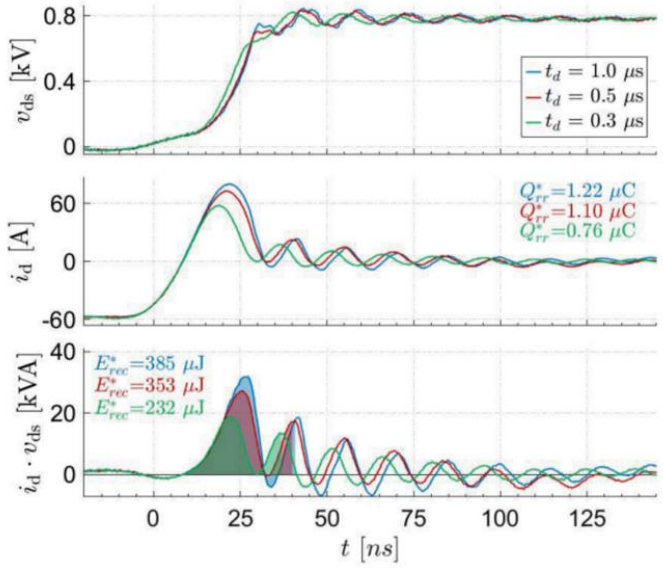
Note: values calculated from datasheets. The graphs reports the best devices among the ones analized

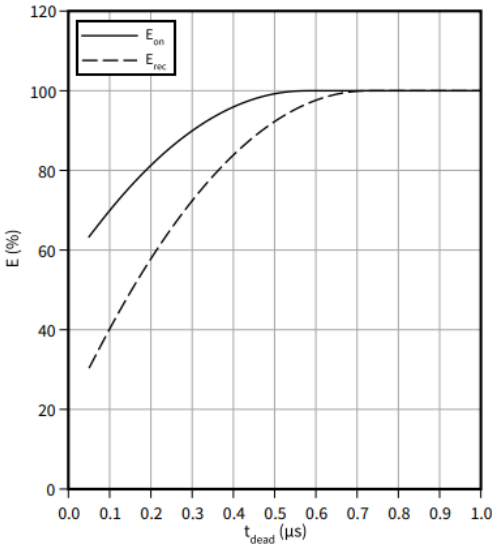
Effect of Deadtime on Switching Loss of SiC MOSFET

- In the SiC MOSFET bridge structure, the longer the deadtime the greater the switching loss
  - SiC PN diode takes longer time to complete equilibrium than Si diode
  - Initial voltage barrier is high and it gradually decreases



$$E_{tot} = \boldsymbol{E_{on}} + \boldsymbol{E_{rr}} + E_{off}$$





If the conduction time is short, the amount of current flowing through the body diode can be less

Summary

- **$R_{DS(on)}$*Q_{GD} indicates switching performance with equivalent $R_{DS(on)}$**
- **$R_{DS(on)}$*E_{OSS} indicates intrinsic power dissipation with equivalent $R_{DS(on)}$**
  - Related to hard switching applications
  - irreverent switching current
  - Proportional to f_{sw}
- **$R_{DS(on)}$*Q_{OSS} or ($R_{DS(on)}$* $C_{o(tr)}$) indicates intrinsic power dissipation with equivalent $R_{DS(on)}$**
  - Related to soft switching applications
  - Affects to the deadtime for ZVS
- **$1/V_{GS(th)}$*Q_{gd}/Q_{gs} indicates PTO immunity**
- **Optimized deadtime with SiC MSOFET enhances system efficiency significantly**

Q&A


Infineon